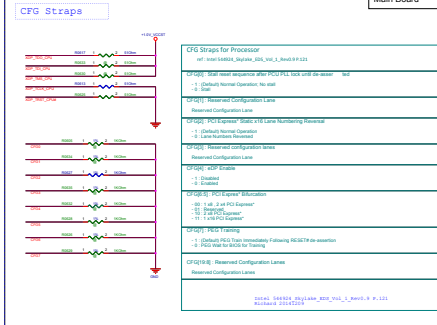
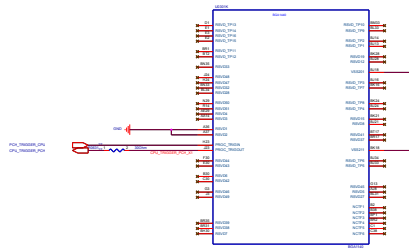
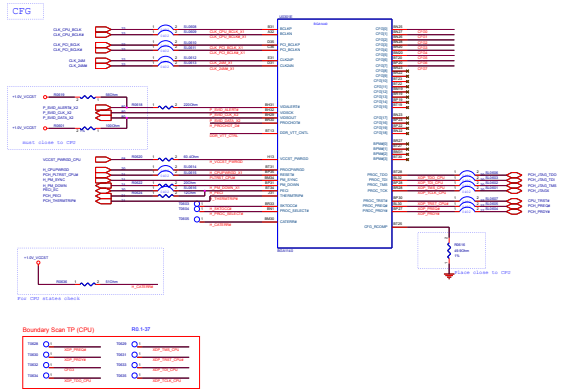


Device Identification		
Device Name: <input type="text"/>		
IMEI	<input type="text"/>	<input type="text"/>
MAC	<input type="text"/>	<input type="text"/>

Case Report Form (CRF)		
Patient Information		
Patient Name	Patient ID Number	
Demographic Data	Age	Sex
Medical History	Current Medications	Previous Treatments
Current Symptoms	Duration of Symptoms	Severity of Symptoms
Physical Examination	Diagnostic Tests	Imaging Studies
Pathology Results	Genetic Testing	Microbiology Results
Therapeutic Response	Adverse Effects	Follow-up Status
Overall Assessment	Prognosis	Recommendations

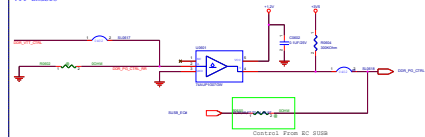
USMCA 2.0 (USMCA 2.0) - Settings			USMCA 2.0 - Settings	
1	USMCA 2.0 (USMCA 2.0) - Settings	↔	1	USMCA 2.0 (USMCA 2.0) - Settings
2	USMCA 2.0 (USMCA 2.0) - Settings		2	USMCA 2.0 (USMCA 2.0) - Settings
3	USMCA 2.0 (USMCA 2.0) - Settings		3	USMCA 2.0 (USMCA 2.0) - Settings
4	USMCA 2.0 (USMCA 2.0) - Settings		4	USMCA 2.0 (USMCA 2.0) - Settings
5	USMCA 2.0 (USMCA 2.0) - Settings	↔	5	USMCA 2.0 (USMCA 2.0) - Settings
6	USMCA 2.0 (USMCA 2.0) - Settings		6	USMCA 2.0 (USMCA 2.0) - Settings
7	USMCA 2.0 (USMCA 2.0) - Settings		7	USMCA 2.0 (USMCA 2.0) - Settings
8	USMCA 2.0 (USMCA 2.0) - Settings		8	USMCA 2.0 (USMCA 2.0) - Settings
9	USMCA 2.0 (USMCA 2.0) - Settings		9	USMCA 2.0 (USMCA 2.0) - Settings
10	USMCA 2.0 (USMCA 2.0) - Settings		10	USMCA 2.0 (USMCA 2.0) - Settings
11	USMCA 2.0 (USMCA 2.0) - Settings		11	USMCA 2.0 (USMCA 2.0) - Settings
12	USMCA 2.0 (USMCA 2.0) - Settings		12	USMCA 2.0 (USMCA 2.0) - Settings
13	USMCA 2.0 (USMCA 2.0) - Settings		13	USMCA 2.0 (USMCA 2.0) - Settings
14	USMCA 2.0 (USMCA 2.0) - Settings		14	USMCA 2.0 (USMCA 2.0) - Settings
15	USMCA 2.0 (USMCA 2.0) - Settings		15	USMCA 2.0 (USMCA 2.0) - Settings



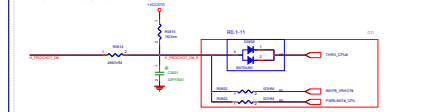


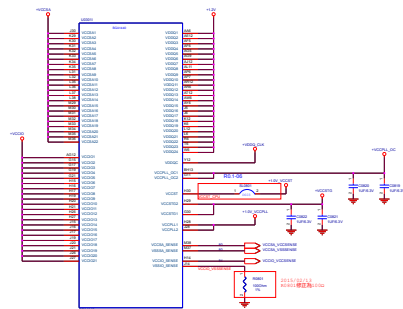
SDR VTT CTRL:
System Memory Power Gate Control:
S1 enables the platform memory VTT regulator
in CB and deeper and S1.
Ref:1544924_144924_0xylake_020_Vol_1_Rev0.9.pdf P.120

VTT Enable



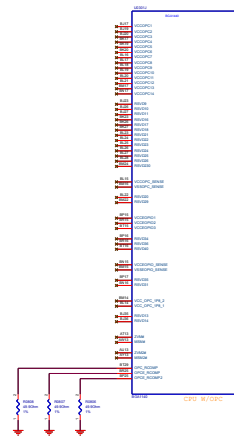
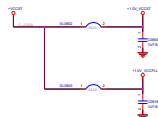
CPU SIDEBAND SIGNALS



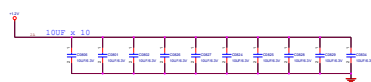


CPU Power Rails

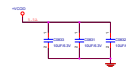
Main Board

+1.0V_VDDQST/+1.0V_VDDQCL
DECAPS Place Back Side (TOP)

+VDDQ DECAPS Place Back Side (TOP)



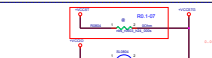
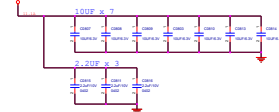
+VDDQ DECAPS Place Back Side (TOP)

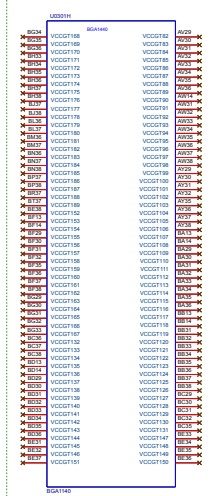
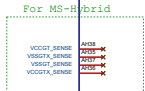


+VDDQ_CLK DECAPS Place Back Side (TOP)

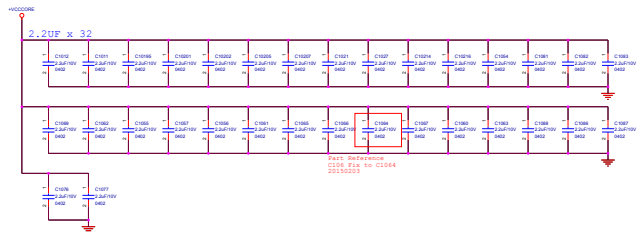
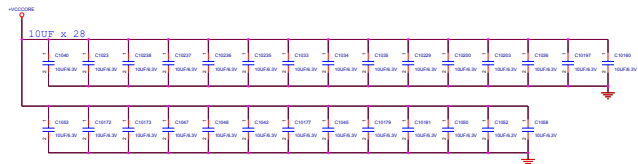


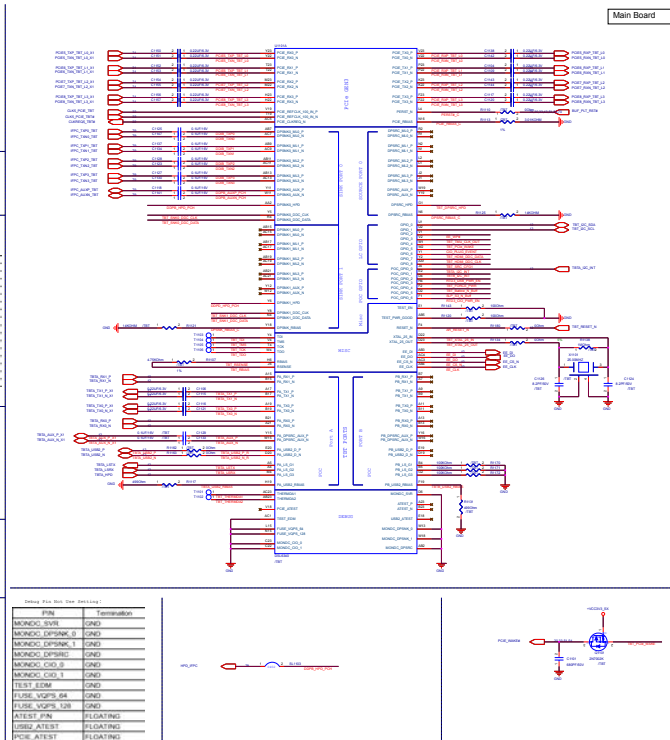
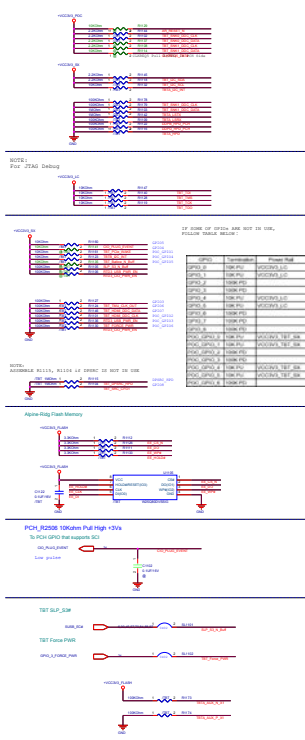
+VDDQ DECAPS Place Back Side (TOP)

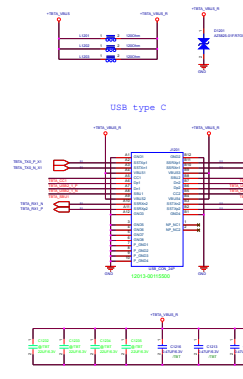
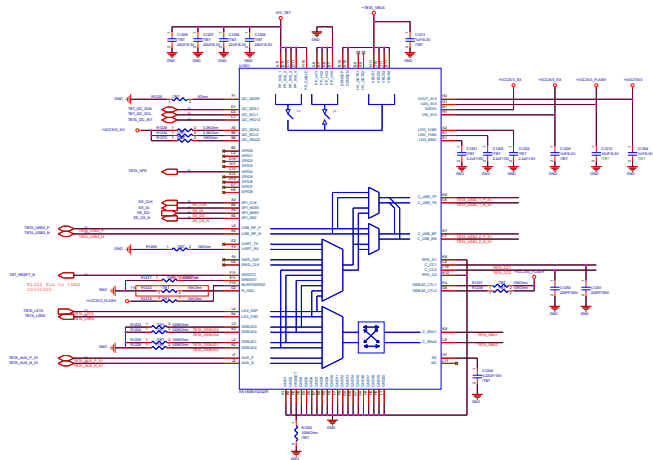
Voltage Segment
+VDDQ is supplied +1.0V (shared with +VDDQSTG)



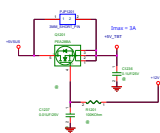
+VCCGT DECAPS Place Back Side (TOP)



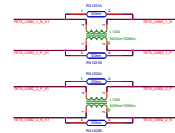
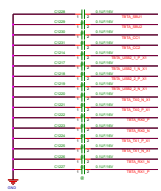


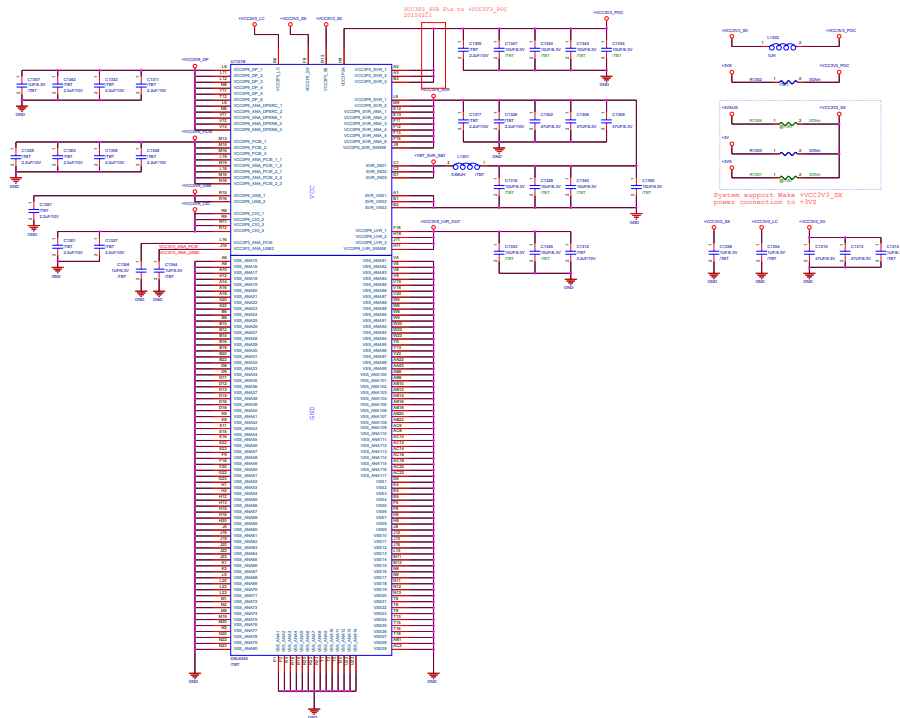


TBT 5V Power



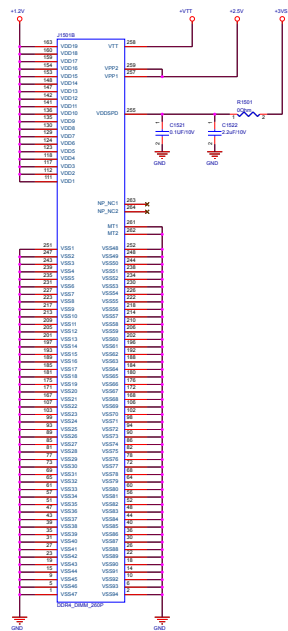
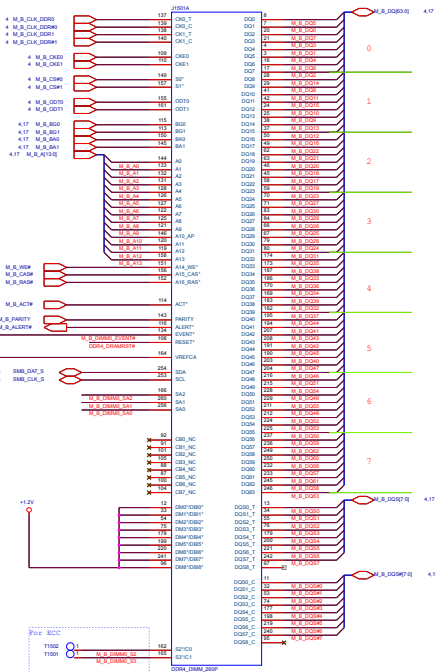
ESD-Protection





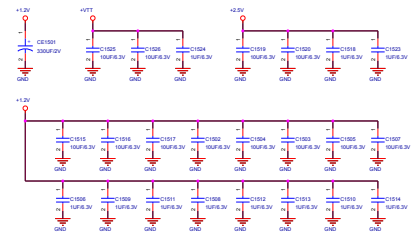
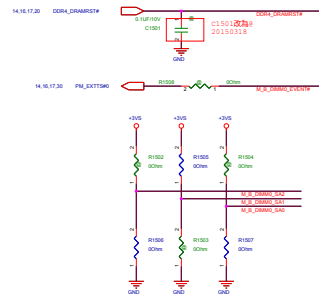
SODIMM CHB-DIMM0
TOP H4.0mm STD (J1501)

12002-00080700
DDR4 DIMM 260P 4H STD



SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

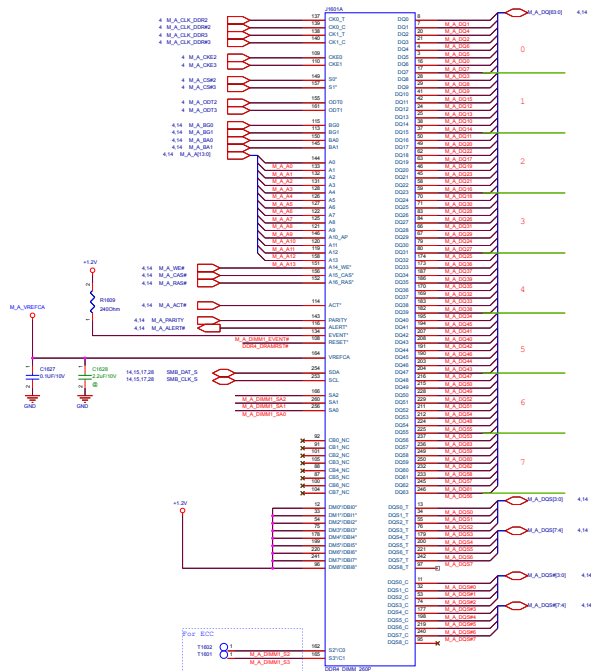
EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH



Main Source	1th FWR	2nd FWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From PUS600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSX	+3VS
		+2.5V

SODIMM CHA-DIMM1
BOT H4.0mm STD (J1601)

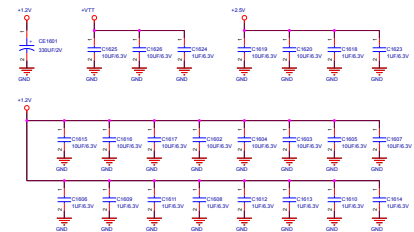
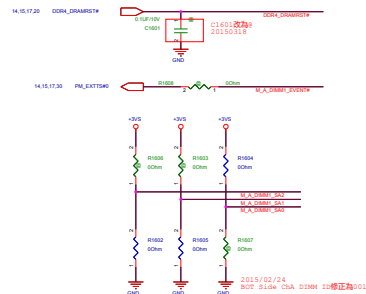
12002-00080700
DDR4 DIMM 260P 4H STD



SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.

SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PC

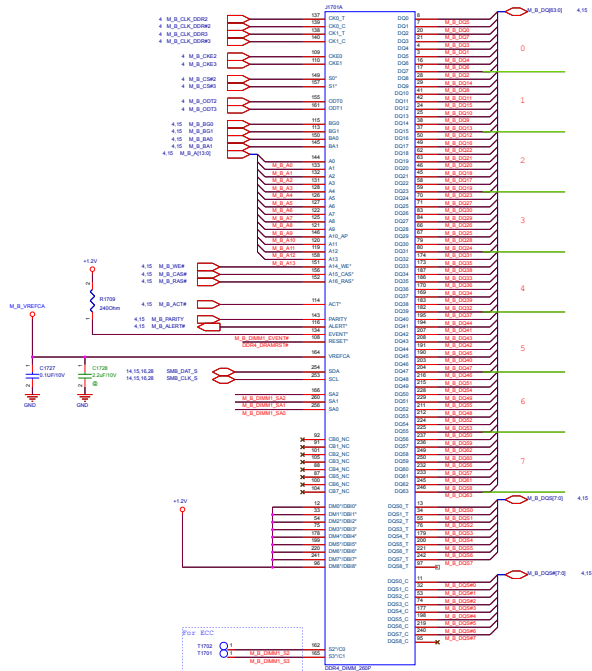


Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From PU8600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

		Project Name: G752VSK		Rev: R2.0
Title: DIM_DDR4 SO-DIMM A0				
Size: Custom	Dept.: ASUSTek COMPUTER INC.	Engineer: Ashton_yang		

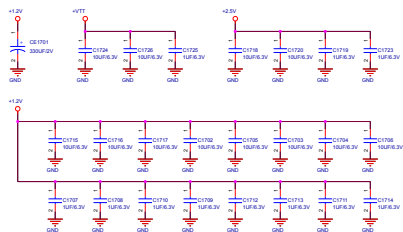
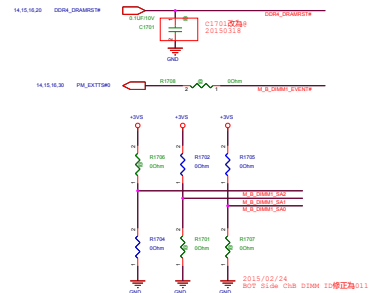
SODIMM CHB-DIMM1
BOT H8.0mm STD (J1701)

12002-00080500
DDR4 DIMM 260P 8H STD



SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired.
SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCB



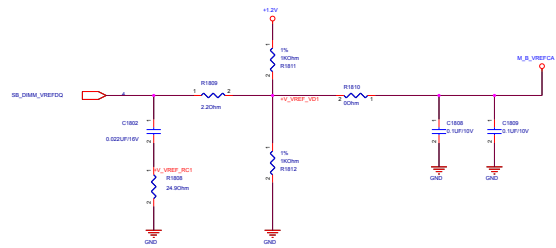
Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From F08600)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

The schematic diagram illustrates the termination circuit for the DDR3 VREF_DQ signal. It features a 25 ohm resistor connected to the VDDQ supply. This resistor is followed by a node that splits into two parallel paths. Each path consists of a 1k ohm resistor in series with a 25 ohm resistor. The top path is connected to the VREF_CA pin of Channel A (DDR4 SO-DIMM), and the bottom path is connected to the VREF_CA pin of Channel B (DDR4 SO-DIMM). A legend at the bottom right defines the symbols: a zigzag line represents 0 Ohm, and a parallel line represents infinity.

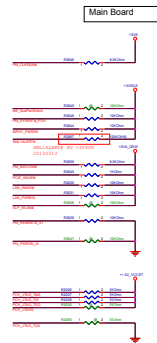
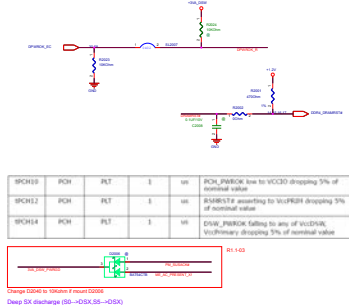
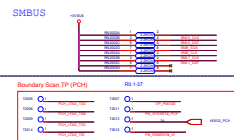
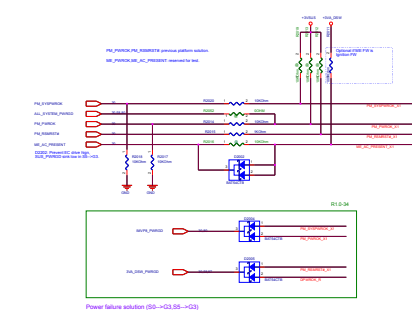
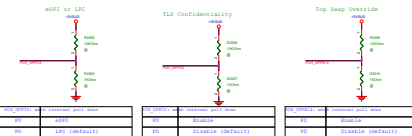
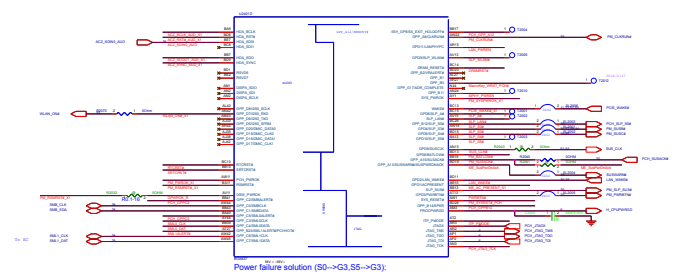
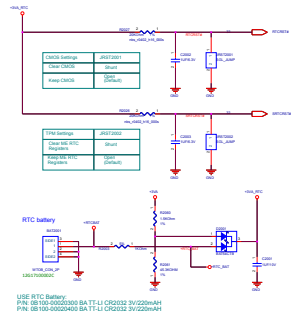
The diagram illustrates the test setup for the DDR3L SO-DIMM. It shows a SKL-H/S processor connected to two DDR3L SO-DIMM modules. The processor's DDR*_VREF_DQ and DDR*_VREF_CA pins are connected to the VREF_DQ and VREF_CA pins of the DIMM connectors. The DIMM connectors are also connected to VREF_DQ and VREF_CA pins of another set of DIMM connectors. The VREF_DQ and VREF_CA pins are connected to a 2.0V VREF supply through a 22kΩ resistor and a 25kΩ resistor. The VREF supply is connected to a 2.0V VREF supply through a 22kΩ resistor and a 25kΩ resistor.

Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	M_A_VREFCA (0.6V From +1.2V)

SO-DIMM Vref

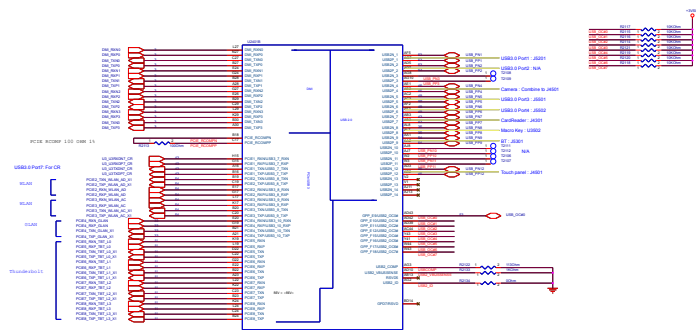


Main Source	1st PWR	2nd PWR	3rd PWR	4th
WCC2B07	+05V_BAT	+10V_B2C		
AC_BAT_212	+1.0VDD05	+VCC02T	+1.0V_VCC02T	
	+1.2V			
	+300V	+30V	+30V_B2C	
	+30V_05W	+3VDD05_PCH	+3VDD05_PCH	+VCC3PA212
	+30V			



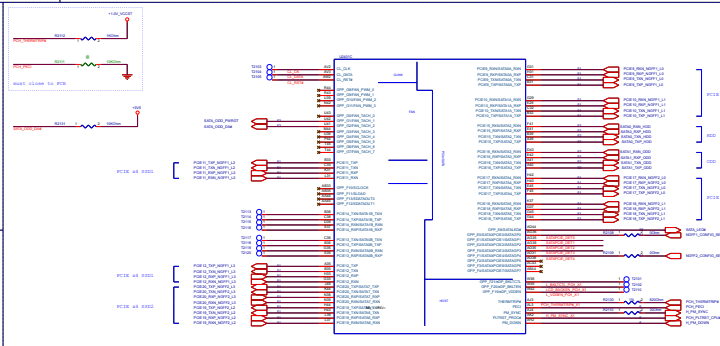
HSIO Setting

SKL, PCI-H C236				SKL, G75 IVC PCI-E CLK Define			
HSIO Default		Function		PCI-E CLK		SRC	
0	PCI02 (From CPU)		iGPU				SRC0
1	USB3 #1						
2	USB3 #2	SSIC #1					
3	USB3 #3	SSIC #2					
4	USB3 #4						
5	USB3 #5						
6	USB3 #6						
7	USB3 #7	PCI-E #1					
8	USB3 #8	PCI-E #2					
9	USB3 #9	PCI-E #3					
10	USB3 #10	PCI-E #4					
11	PCI-E #5	PCI-E					
12	PCI-E #6						
13	PCI-E #7						
14	PCI-E #8						
15	PCI-E #9	SATA #0	Q46				
16	PCI-E #10	SATA #1	Q46				
17	PCI-E #11						
18	PCI-E #12	Q46					
19	PCI-E #13	SATA #0*	Q46				
20	PCI-E #14	SATA #1*	Q46				
21	PCI-E #15	SATA #2					
22	PCI-E #16	SATA #3					
23	PCI-E #17	SATA #4					
24	PCI-E #18	SATA #5					
25	PCI-E #19	SATA #6					
26	PCI-E #20	SATA #7					

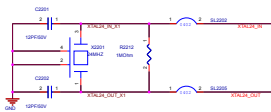


USB Setting

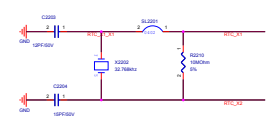
SKL, G75 IVC USB2 & USB3 Define			
USB2	Function	USB2	Function
USB2 #1	USB IO(USB3_0)	USB2 #1	USB IO(USB3_0)
USB2 #2		USB2 #2	
USB2 #3		USB2 #3	
USB2 #4	Camera	USB2 #4	3D Camera
USB2 #5	USB IO(USB3_2)	USB2 #5	USB IO(USB3_2)
USB2 #6	USB IO(USB3_3)	USB2 #6	USB IO(USB3_3)
USB2 #7	USB Card Reader	USB2 #7	USB Card Reader
USB2 #8	Macro Key	USB2 #8	
USB2 #9	BT	USB2 #9	
USB2 #10		USB2 #10	
USB2 #11		USB2 #11	
USB2 #12	Touch Panel	USB2 #12	
USB2 #13		USB2 #13	
USB2 #14		USB2 #14	



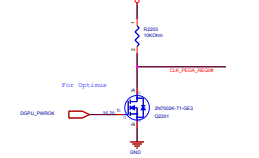
XTAL 24MHz



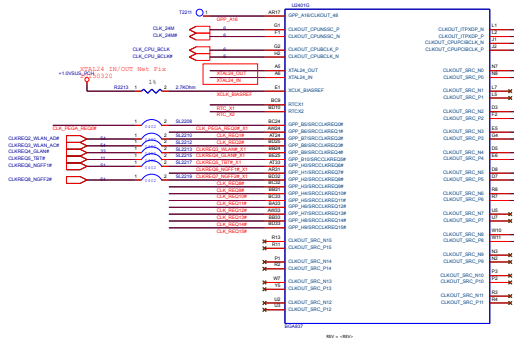
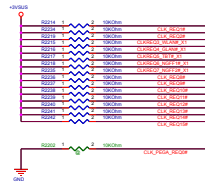
RTC CRYSTAL 32.768KHz



DGPU CLKREQ#



PCH CLKREQ Setting:



USB10 Port1 : J5001

USB10 Port2 : N/A

USB10 Port4 : J5002

USB10 Port3 : J5001

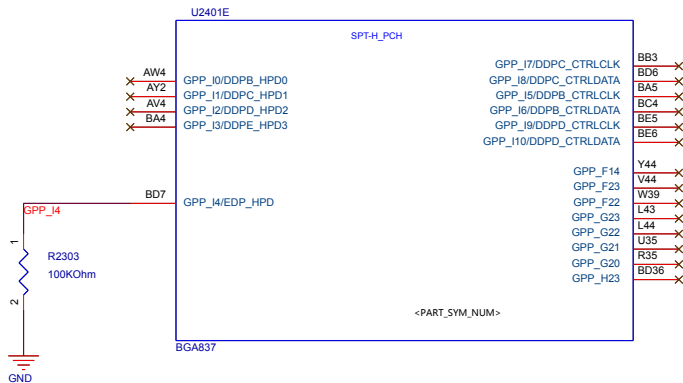
LPC_A00

LPC_A00


LPC_A00

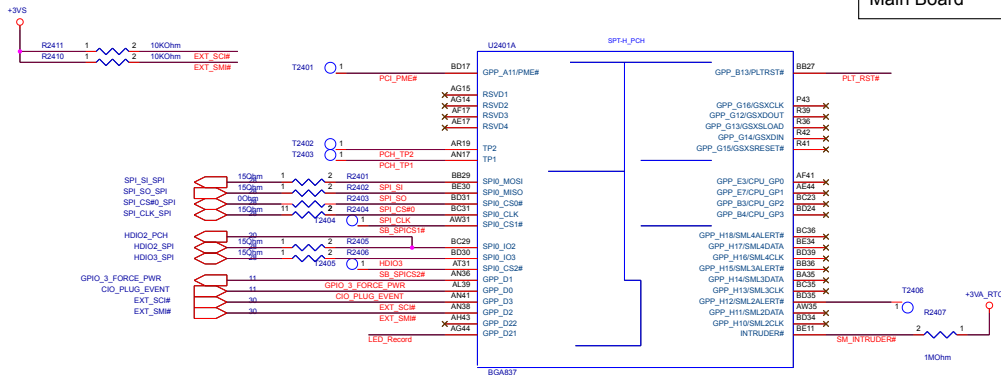
LPC_A00

DDPD Strap Setting Update :
 0 = Port D is not detected (Default)
 1 = Port D is detected
 20150309



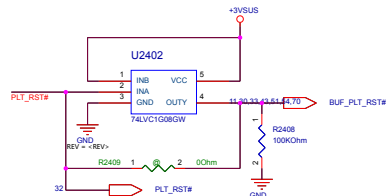
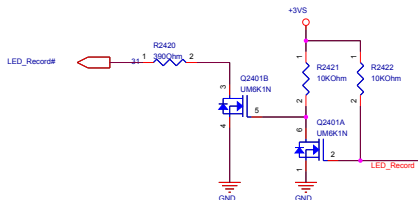
REV = <REV>


		Project Name	Rev
		G752VSK	R2.0
Title : PCH-CPT(4)_C801,PCI,DP			
Size A	Dept.: ASUSTeK COMPUTER INC.	Engineer:	Ashton_yang
Date: Wednesday, October 12, 2016	Sheet	23	of 102

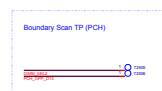
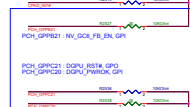
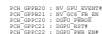


Record Key LED Control Circuit

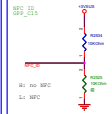
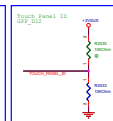
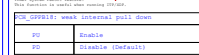
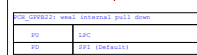
LED Record# of Current :
 $(5 - 2.35) / 390 = 6.8\text{mA}$

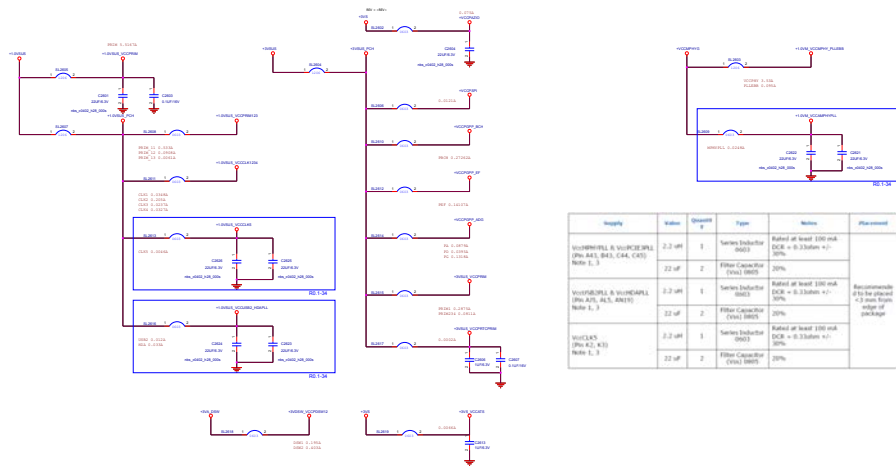
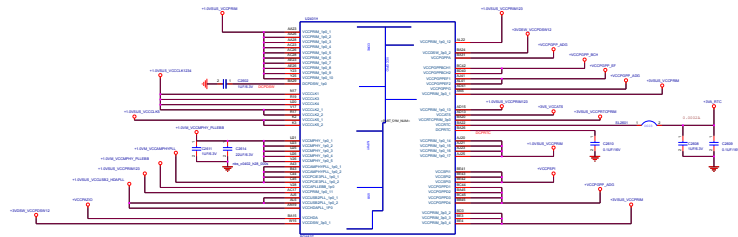


		Project Name G752VSK		Rev R2.0
Title : PCH-CPT(5)_LPC,SPI,SMBUS				
Size A	Dept.: ASUSTek COMPUTER INC.		Engineer: Ashton_yang	
Date: Wednesday, October 12, 2016		Sheet	24	of 102

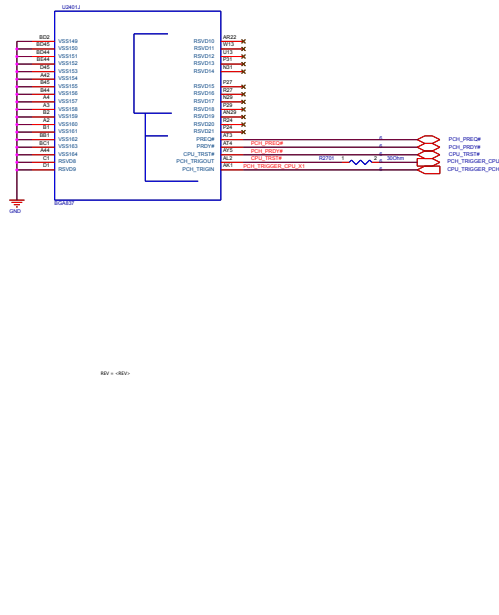


	PCR_ID0	PCR_ID1
Disable GC6	L	L
Enable GC6	L	R





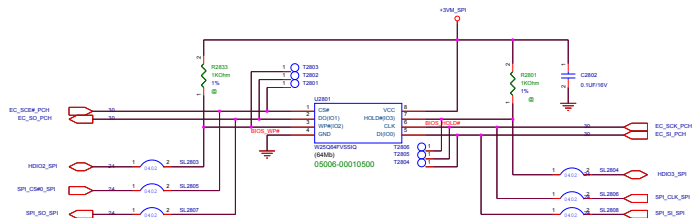
Supply	Value	Quantity	Type	Notes	Plan comment
VOUGR01LA & VOUGR01LA (Pn A43, B43, C44, C45) Refer 1, 3	2.2 off	1	Series Inductor (MS03)	Rated at least 100 mH DCR = 0.33 ohms +/- 30%	
	22 off	2	Filter Capacitor (C10)	20%	
VOUGR01LA & VOUGR01LA (Pn A43, A45, A4615)	2.2 off	1	Series Inductor (MS03)	Rated at least 100 mH DCR = 0.33 ohms +/- 30%	
Refer 1, 3	22 off	2	Filter Capacitor (C10) (MS05)	20%	Replacements to be placed in the edge of package
VOUGR01S (Pn A42, K3)	2.2 off	1	Series Inductor (MS03)	Rated at least 100 mH DCR = 0.33 ohms +/- 30%	
Refer 1, 3	22 off	2	Filter Capacitor (C10) (MS05)	20%	



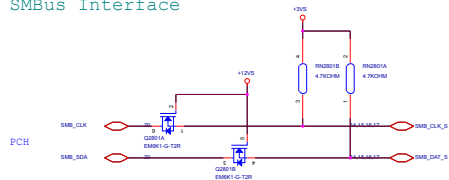
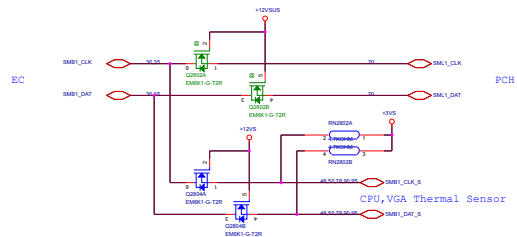
1st SPI ROM

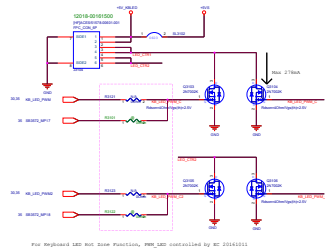


Main: 05006-00010500 (fixed quad bit)

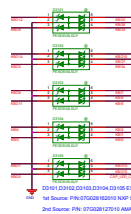


SMBus Interface





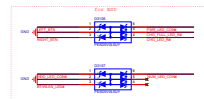
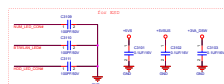
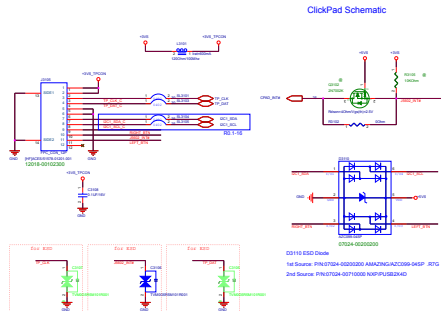
For Keyboard LED Hot Swap Function, PWM_LED controlled by XT 20161011



Macro Key	KG Backlight	Macro Key LED Behavior
J104_Pin1 LED_Combine	J104_Pin1 RGB_LED_PinM	Combine_Key(2,3,4)
No Set (0)	No Set (0)	LED OFF (0)
No Set (0)	Set (1)	LED OFF (0)
Set (1)	No Set (0)	Flash, then LED OFF(0)
Set (1)	No Set (0)	Flash, then LED ON(1)

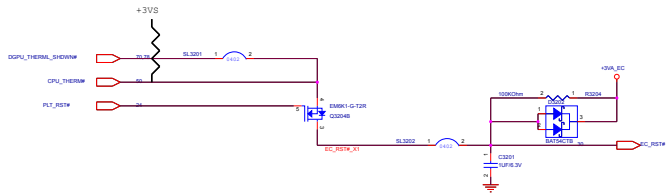
To Touchpad

To Touchpad Button

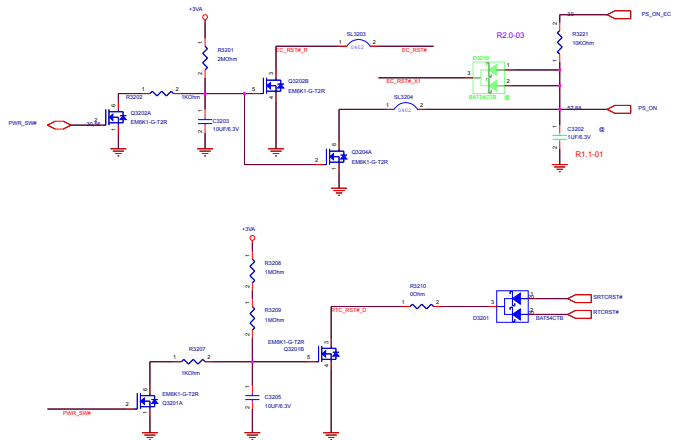


2nd Source: PIN: 07G028127010 AMAZING: SCT0-01

EC Reset Circuit



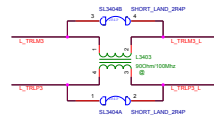
battery embedded (press pwr_sw 10sec, then reset ec)





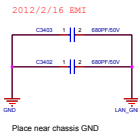
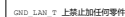
1st Source: P/N:12014-00161700 FOXCONN/JM361 1-NS640003-7H

2nd Source: P/N:12014-00035500 SINGA TRON/2RJ1648-000111F

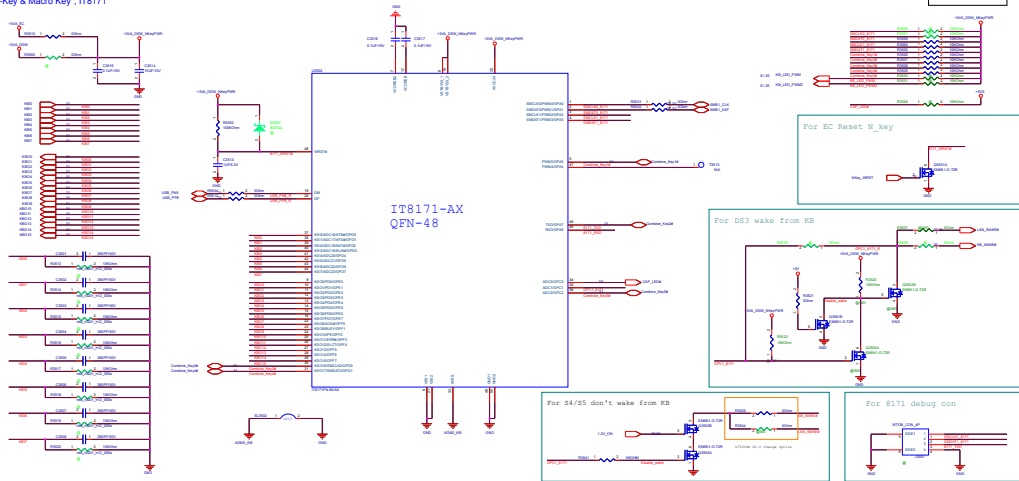


1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP .R7G

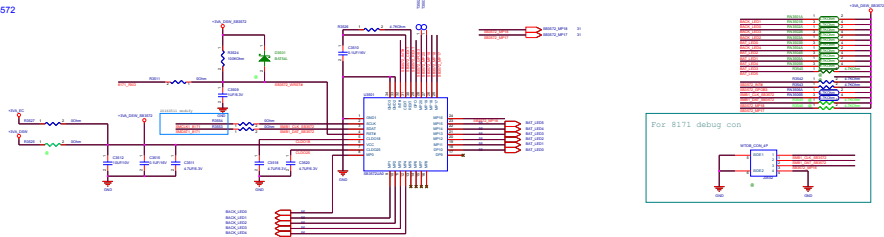
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

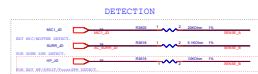
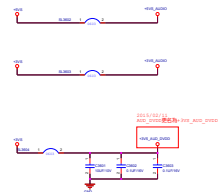
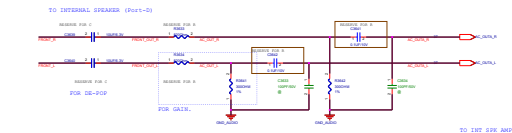


N-Key & Macro Key , IT8171

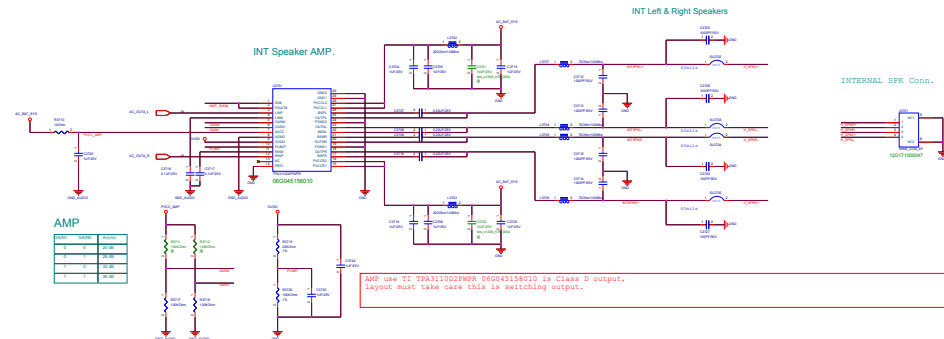


Light Bar , SB3572

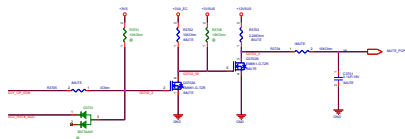




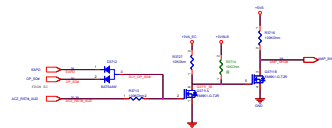
Main Board



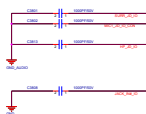
EXT JACK MUTE CONTROL



INT SPK MUTE CONTROL



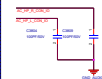
For EMI



HP & SPDIF DETECT RULE

	IN 5	IN 4	IN 3
HPDET_HP	LOW	LOW	LOW
HPDET_SPD	LOW	LOW	LOW
HPDET_DET	LOW	LOW	LOW

For EMI



2013/01/18 NAKSOLUR
Fix HP PDP Noise issue in Response S3.
Change Power plan from <15V5G to <15V A.

For EMI

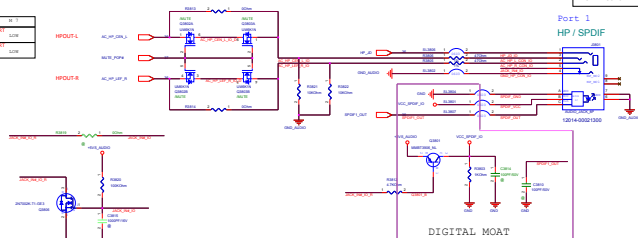
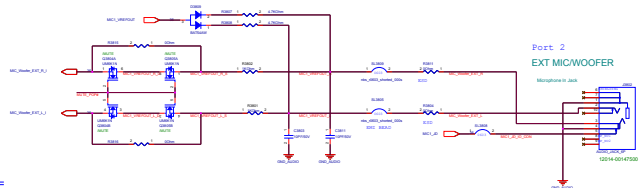
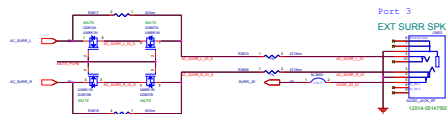


2013/01/18 NAKSOLUR
Fix PDP Noise issue in Response S3.
Change Power plan from <15V5G to <15V A.

For EMI



Main Board

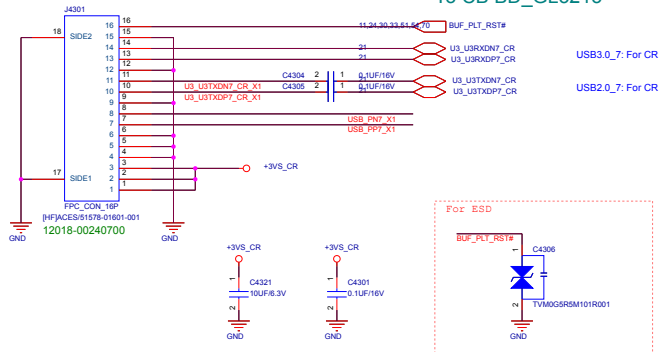
Port 1
HP / SPDIFPort 2
EXT MIC/WOOFERPort 3
EXT SURR SPK



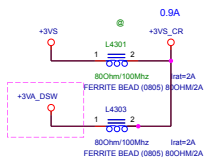
CR I/O Conn. (MB)

Main Board

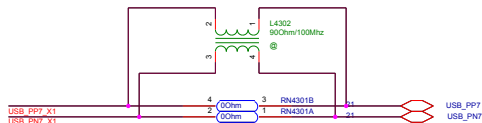
To CB BD_GL3213



CardReader PWR

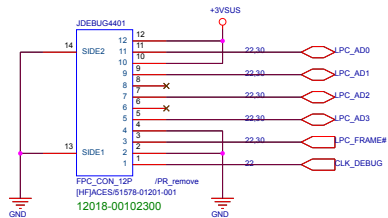


For EMI



ASUS		Project Name	Rev
G752VSK			R2.0
Title : CB IO CON			
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: Ashton_yang
A			
Date: Wednesday, October 12, 2016	Sheet	43	of 102

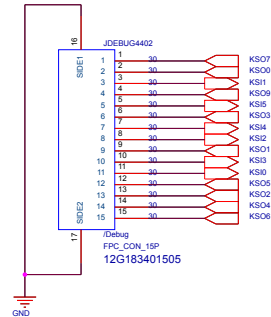
LPC Debug Port



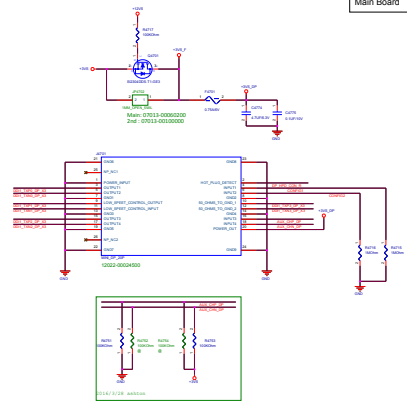
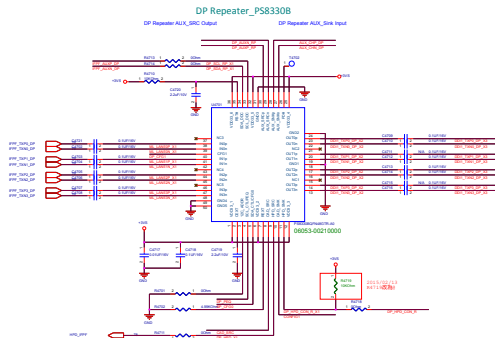
JDEB4401 Connector (MP USE)

1st Source: P/N:12018-00102300 ACES/51578-01201-001

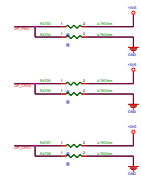
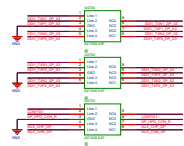
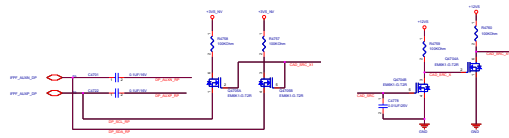
2nd Source: P/N:12018-00102100 ENTER Y/6705K-Y12N-00L

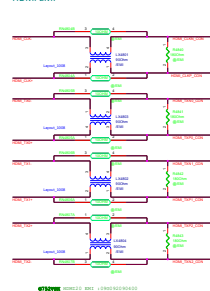
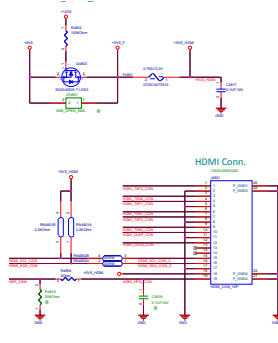
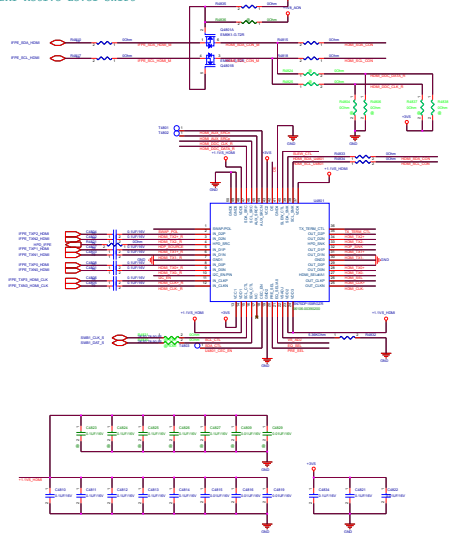
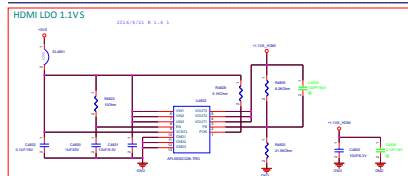


Project Name		Rev
ASUS G752VSK		R2.0
Title : BUG NewCard & LPC		
Size	Dept.: ASUS&K COMPUTER INC.	Engineer: Ashton_yang
Date: Wednesday, October 12, 2016	Sheet	44 of 102



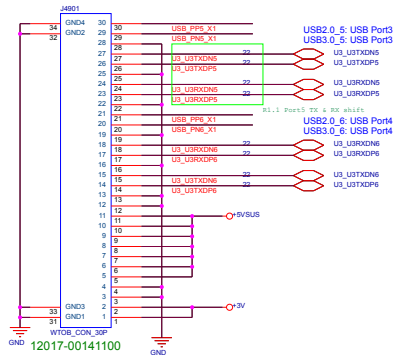
2014/3/28
BIOSTAR A62-0.00 reference Pseudo Design Circuit PS8330B
Pin MUX2P To MUX2 Single No Display Issue



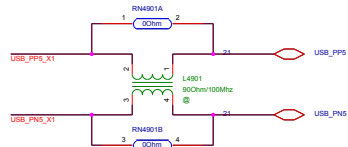


Main Board

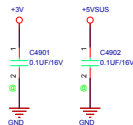
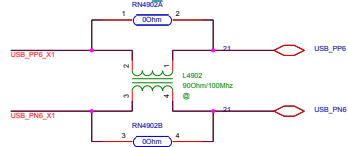
To USB3.0 I/O Board (PAGE55)



USB3.0 Port3_J5501

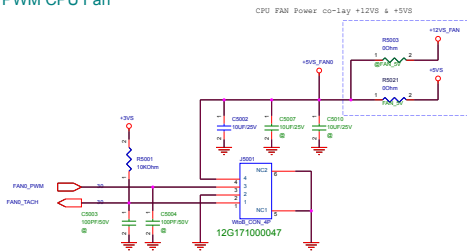


USB3.0 Port4_J5502



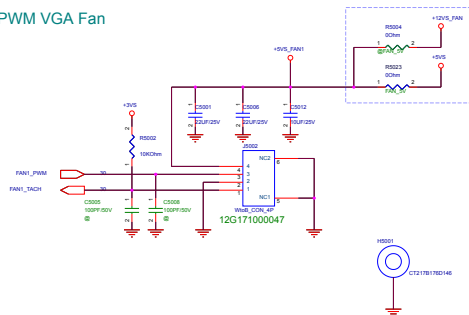
ASUS		Project Name	Rev
G752VSK			R2.0
Title: USB3.0 IO CON			
Size	Dept.: ASUS&K COMPUTER INC.	Engineer:	Ashton yang
A			
Date: Wednesday, October 12, 2016	Sheet	49	of 102

PWM CPU Fan

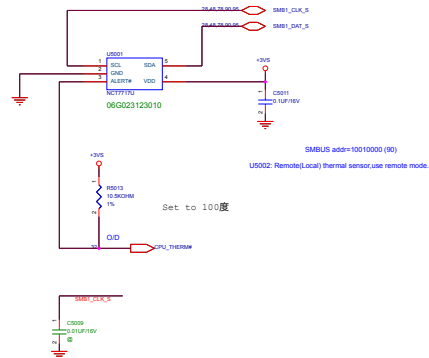


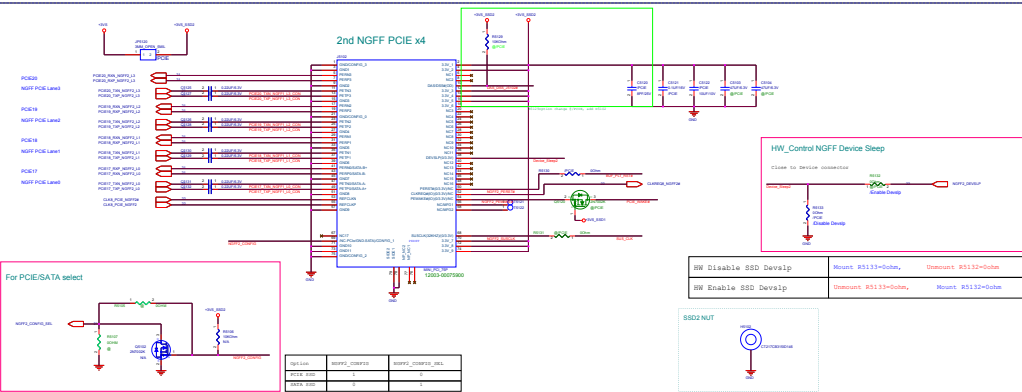
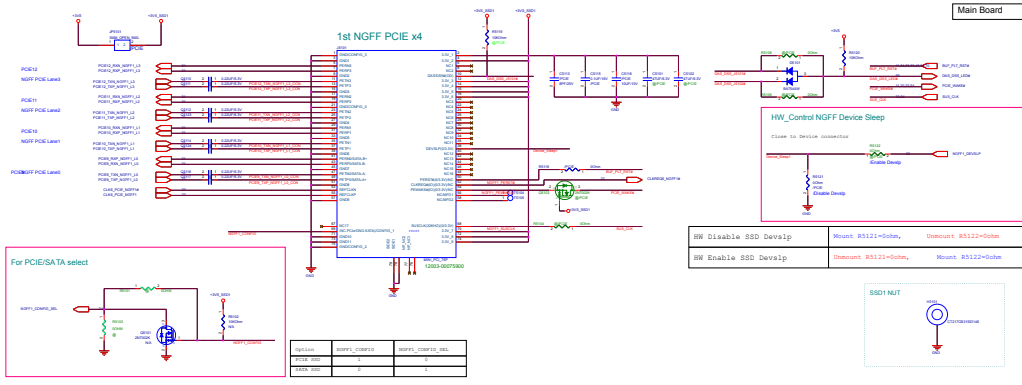
GPU FAN Power co-lay +12VS & +5VS

PWM VGA Fan



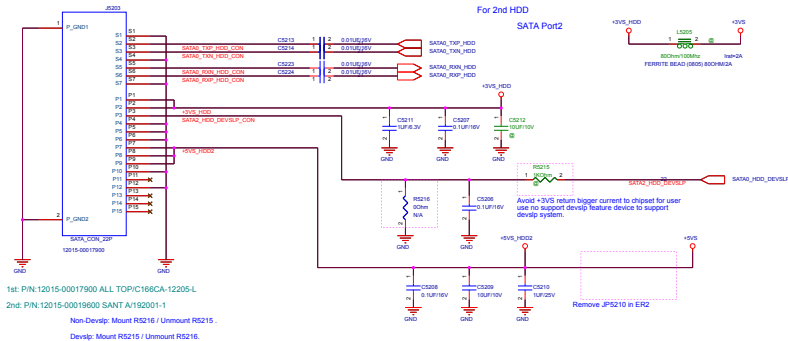
CPU Thermal Sensor





Main Board

2nd HDD



EMI Request



1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F

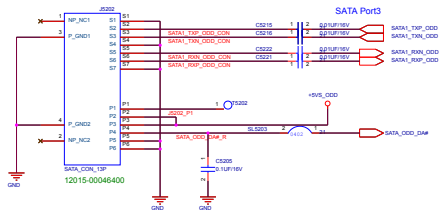
2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

For RF requirement

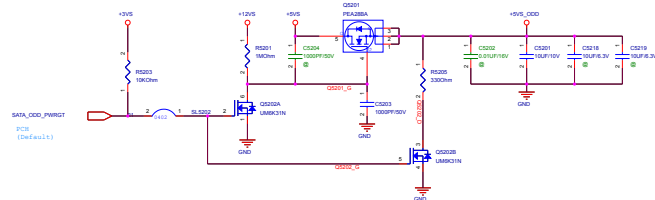
EMI Request0520



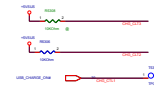
ODD



ODD Power



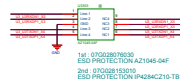
USB Charge Circuit (For PORT 1)



HCW, BCW Platform : Unmount Rds

		11264h / 11268h				
CHG_CIL		[1]	[0]	[4]		
USB_CHARGER_On#	0	0	1	1	AUTO	
	1	1	1	1	CDP	
USB_CHARGE_DISABLE		0	1	1	0	SDP

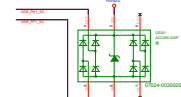
USB3.0 ESD-Protection



BC1.2 Charger Disable

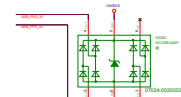


USB2.0 ESD-Protection



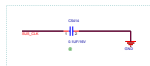
1st Source: PIN:07024-00000200 AMAZING!AZC099-046P .R7G

2nd Source: P/N:07024-00710000 NXP/PU5B2K4D



1st Source: PIN:07024-00200200 AMAZING!AZC099-045P .R7C

2nd Source: P/N:07034-00710000 NXP/PU5BZX4D



1st Source: P/N:12003-00071300 KYOCERA/20541 1007101894E
2nd Source: P/N:12003-00074900 ACES/51746-0675P-005
3rd Source: P/N:12003-00076000 ARGOSY/NAGE0-S6701-TP20

Alt. Source: D.91-12003-00022-000, JACUS4832507U2-05AR

76	RESEARCH	RESEARCH	76
77	RESEARCH	RESEARCH	77
78	RESEARCH	RESEARCH	78
79	RESEARCH	RESEARCH	79
80	RESEARCH	RESEARCH	80
81	RESEARCH	RESEARCH	81
82	RESEARCH	RESEARCH	82
83	RESEARCH	RESEARCH	83
84	RESEARCH	RESEARCH	84
85	RESEARCH	RESEARCH	85
86	RESEARCH	RESEARCH	86
87	RESEARCH	RESEARCH	87
88	RESEARCH	RESEARCH	88
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90	RESEARCH	RESEARCH	90
91	RESEARCH	RESEARCH	91
92	RESEARCH	RESEARCH	92
93	RESEARCH	RESEARCH	93
94	RESEARCH	RESEARCH	94
95	RESEARCH	RESEARCH	95
96	RESEARCH	RESEARCH	96
97	RESEARCH	RESEARCH	97
98	RESEARCH	RESEARCH	98
99	RESEARCH	RESEARCH	99
100	RESEARCH	RESEARCH	100

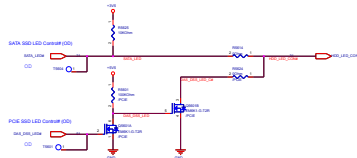
To switch WNGD, level, low
 RT take up to ground
 time if use
 +VCC, RT change to +VCC
 RT can work quickly when
 RT change on.

SUS PWR

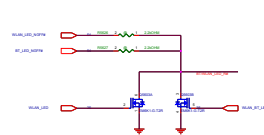
Project which use the
combo card schematic
should
make sure that BT CN
signal can't be HIGH at
E1/E4/E5 state to prevent
damage.

HEAD:
CT 21 TW 070244E
13GNSZ 10M025-1
LOCKED IN LAM CARO N
also sent Aug 2008

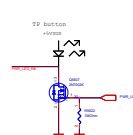
HDD LED & PCIE SSD LED



BT/WLAN LED Control

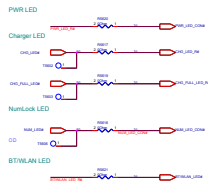


PWR LED Control

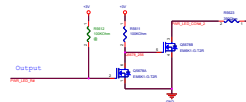


Main Board

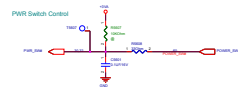
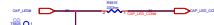
To TP Button CONN



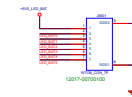
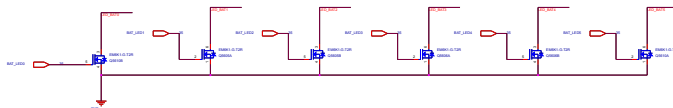
OS LED Control



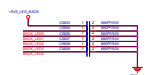
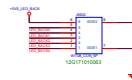
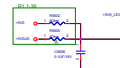
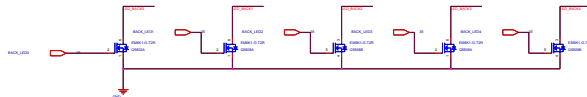
To Power Button IO BD

To Keyboard CONN
CapsLock LED

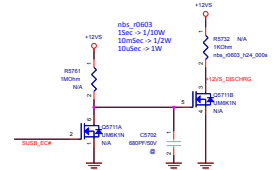
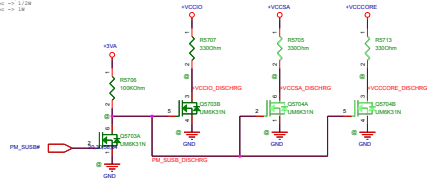
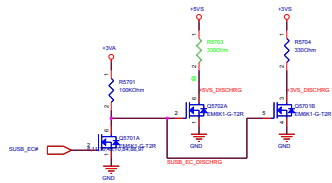
To LED BAT BAR



To LED BACK BAR



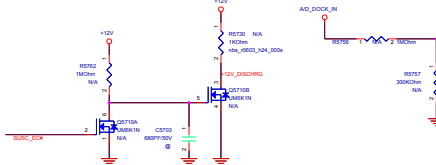
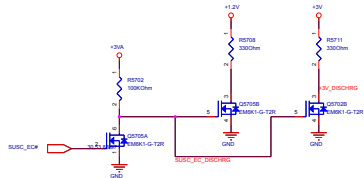
Main Board



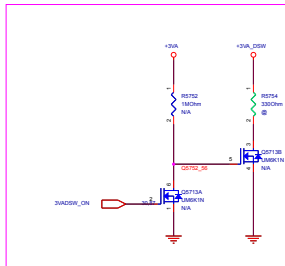
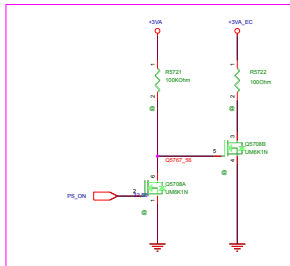
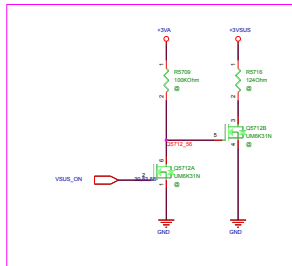
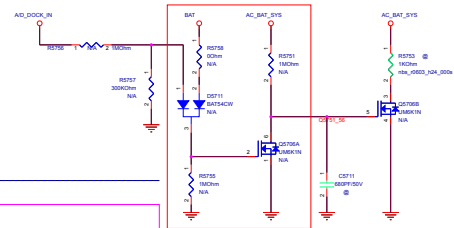
+12V & +12V5 需保持 +12V5 0.5W 才能正常

bsa_v0403
15mSec -> 1/10W
10mSec -> 1/2W
10uSec -> 1W

SUSC_EC# turn off discharge before +12V ON
+12V turn on discharge after SUSC_EC# OFF

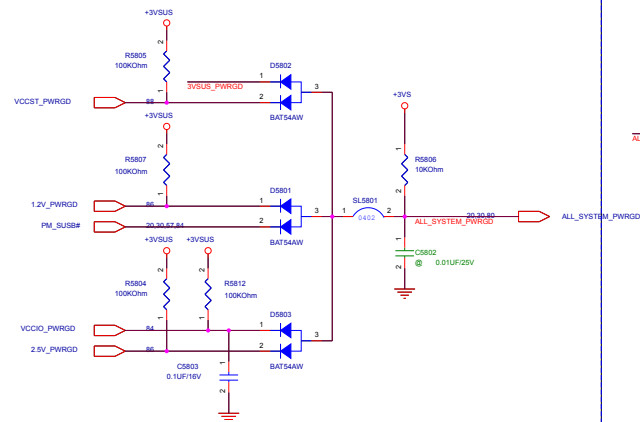
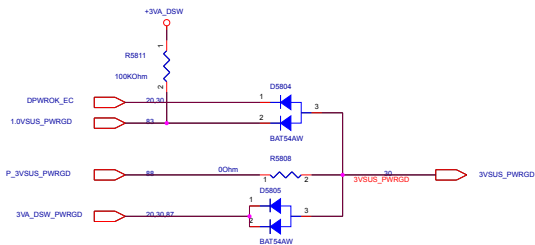


每小時耗 0.45mW
每個月耗 324mW
0.45mW=(15X15/1M)x2

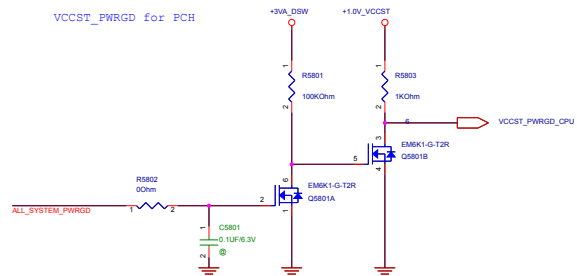


ASUS		Project Name	Rev
G752VSK			RE.0
Title : DSG Discharge			
Size	Dept.:	ASUSTek COMPUTER INC.	Engineer: Ashton_yang
Date: Wednesday, October 12, 2016	Sheet	57	of 102

Main Board



VCCST_PWRGD for PCH



ASUS Project Name
G752VSK

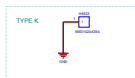
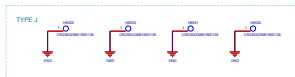
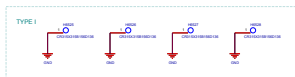
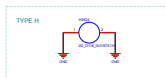
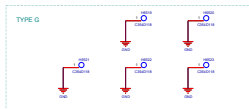
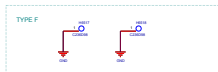
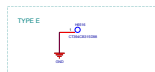
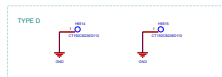
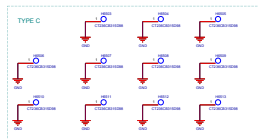
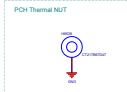
Rev
R2.0

Title : PRO Protect

Size Custom Dept.: ASUS/TEK COMPUTER INC. Engineer: Ashton yang

Date: Wednesday, October 12, 2016 Sheet 58 of 102

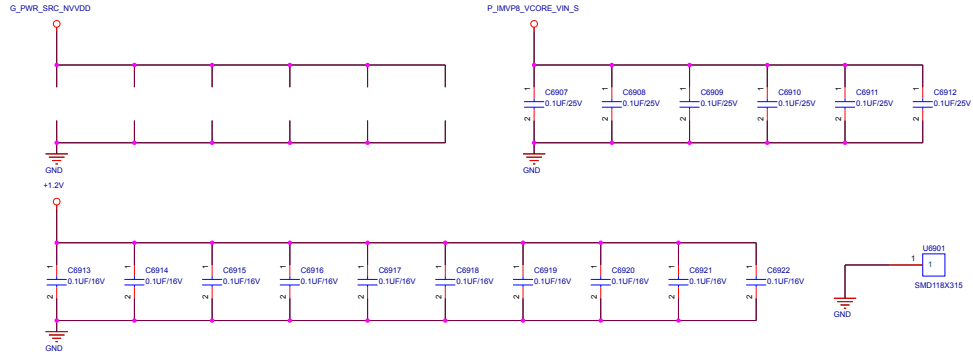
TOP Component



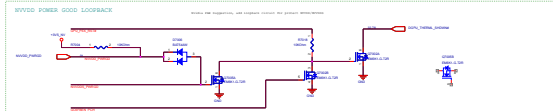
Main Board

BOT Component

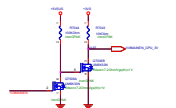
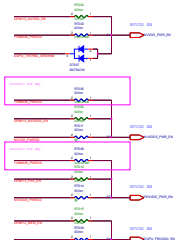
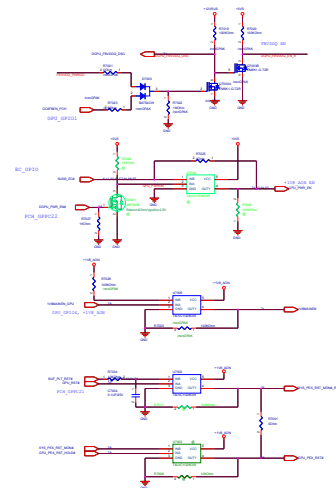
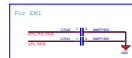
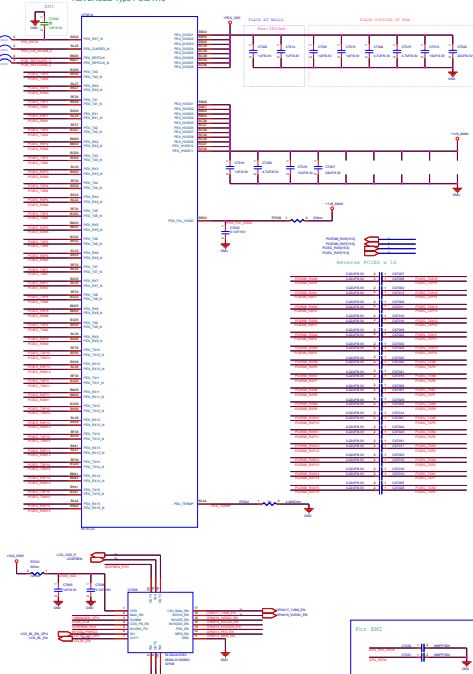
EMI



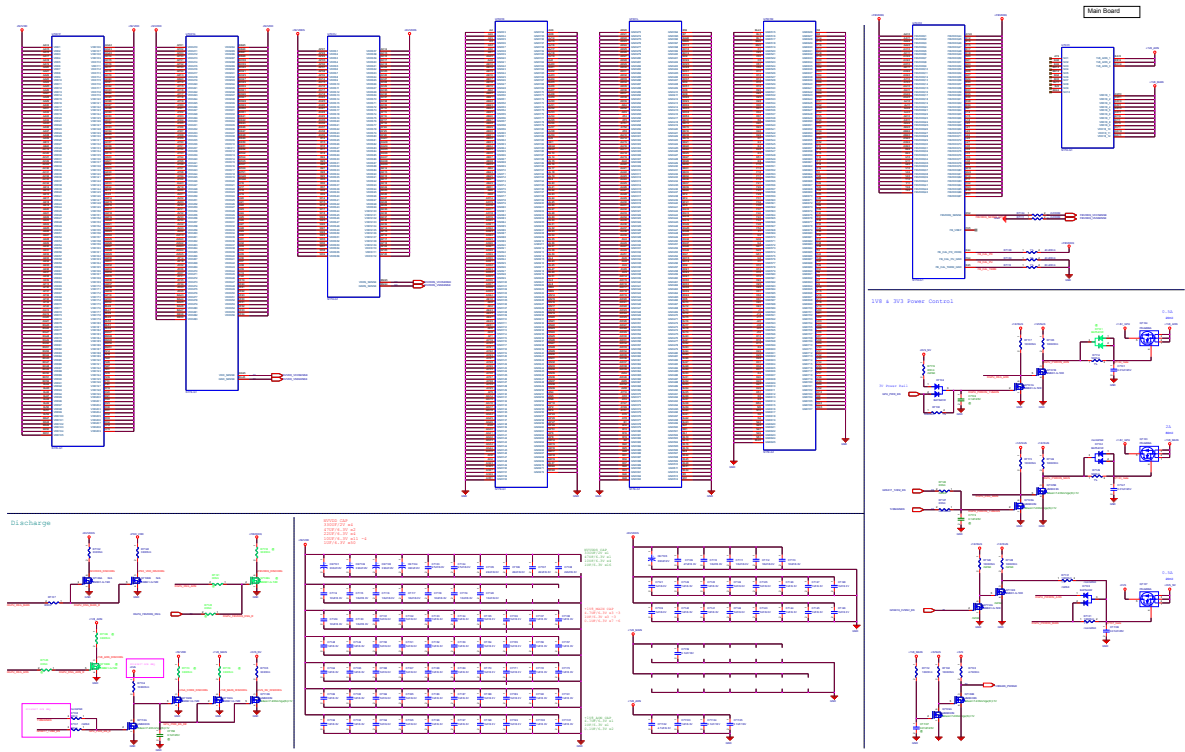
ASUS		Project Name	Rev
		G752VSK	R2.0
Title : OTH EMI CAPS			
Size	Dept.:	ASUSTeK COMPUTER INC.	Engineer: Ashton_yang
A			
Date: Wednesday, October 12, 2016		Sheet	69 of 102



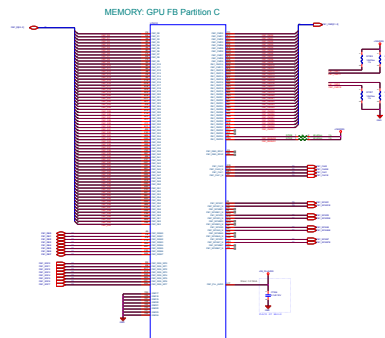
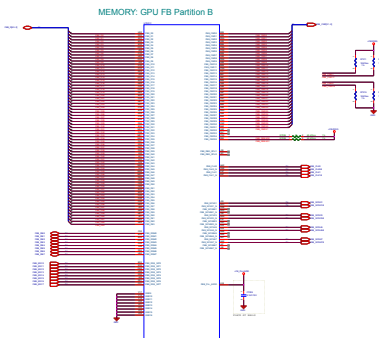
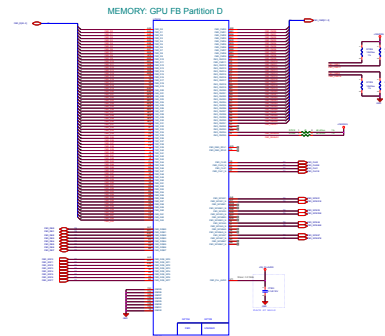
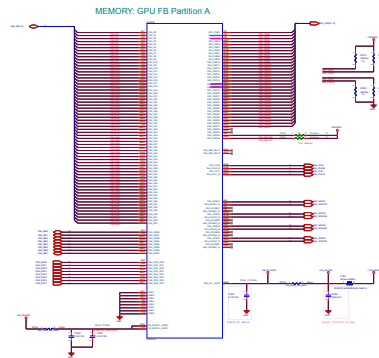
GPU POWER SEQUENCE CONTROL

PCI EXPRESS_Graphics
REVERSED Type PCIe X16

Main Board

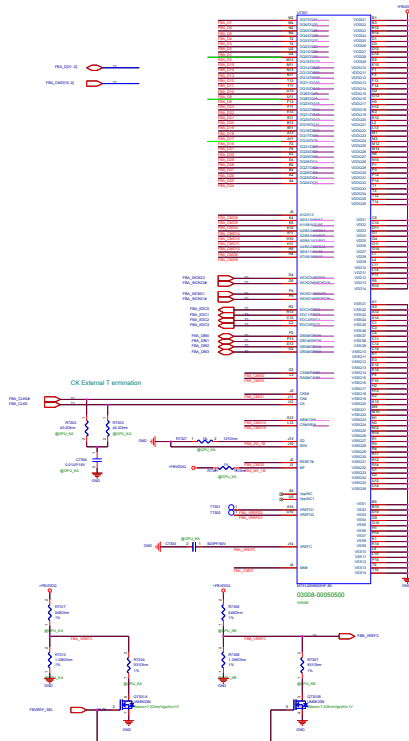


Memory Board



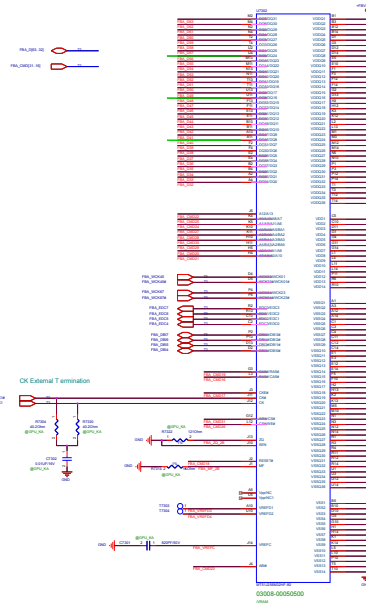
FBA Partition Memory (1 of 2)

MF=1 Mirror



FBA Partition Memory (2 of 2)

MF=0 Normal



R1 3-40 R1 2-22

USE GDS50 VDRAM (2GBx 32 (512MB))

1st: PIN 0308-00030100 HYUNDAI H5G41Q4MFR T2C (M-dw) ,Step: 0 x2

2nd: PIN 0308-00030205 SAMSUNG H5G41325FC H2C3 ,Step: 0x3

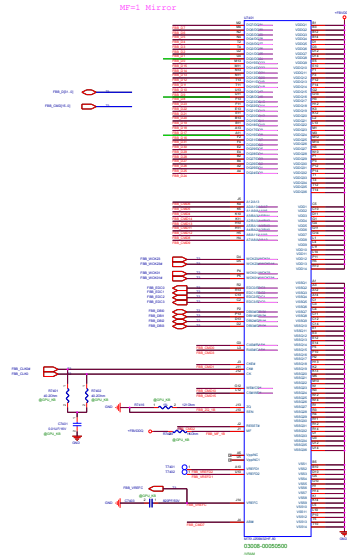
3rd: PIN 0308-00030405 Micron EDW532BAG-03 F (B-dw) ,Step: 0x4

GDS5 MODE SELECTION

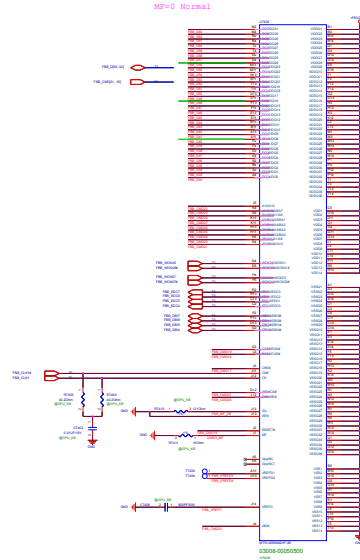
MODE	MF	SW1	SW2
00	0	V000	V000
01	1	V000	V000
02	0	V000	V000
03	1	V000	V000

Main Board

FBB Partition Memory (1 of 2)



FBB Partition Memory (2 of 2)



R1-0.00 R1-0.00

UDK 00000000 00000000 00000000 00000000

1st PIN 00000000 00000000 HYPERMAGNETIC T2C (8-day, 5-day, 0-day)

2nd PIN 00000000 00000000 SAMSUNG MAGNETIC T2C (8-day, 5-day, 0-day)

3rd PIN 00000000 00000000 Mouser Channel (8-day, 5-day, 0-day)

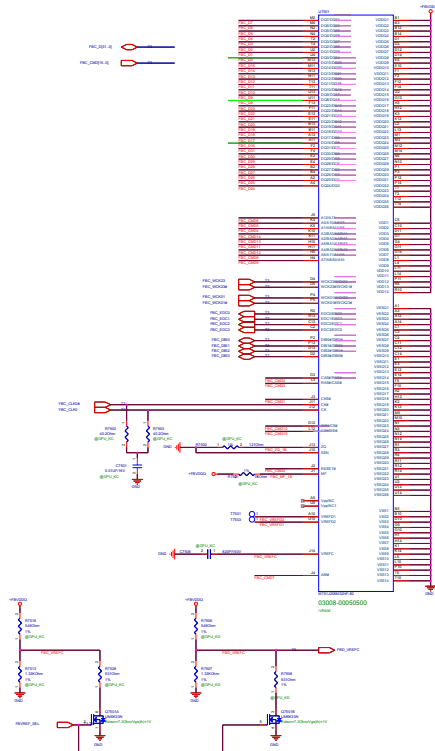
GDD5 MODE SELECTION

MODE	MF	MODE	MODE
0	0	0	0
1	1	1	1
2	2	2	2
3	3	3	3
4	4	4	4
5	5	5	5
6	6	6	6
7	7	7	7
8	8	8	8
9	9	9	9
A	A	A	A
B	B	B	B
C	C	C	C
D	D	D	D
E	E	E	E
F	F	F	F

Main Board

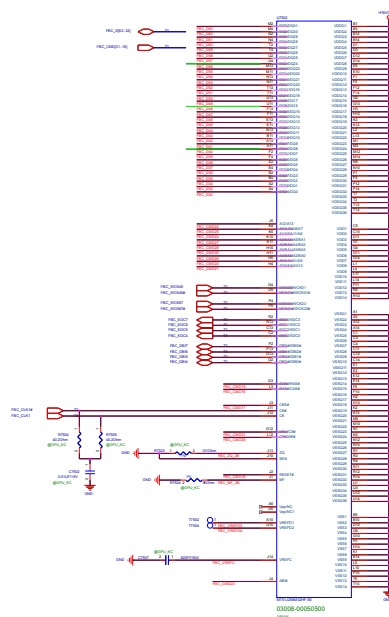
FBC Partition Memory (1 of 2)

MF=1 Mirror



FBC Partition Memory (2 of 2)

MF=0 Normal



P1 3-00 P1 2-05

USE GDDR5 VRAM (2GB x 32 (128MB))

1st PIN 03008-00030100 HYUNDAI H5GQ4MFR-T2C (M-die) (Strap: 0 x2)

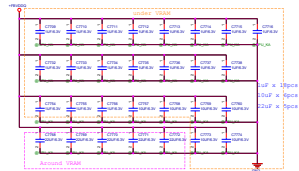
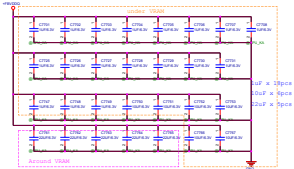
2nd PIN 03008-00030200 SAMSUNG K4G4132PFC H2CS (Strap: 0x3)

3rd PIN 03008-00030400 Micron EDV4323BAG-60-P (B-die) (Strap: 0x4)

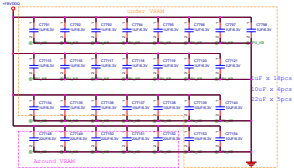
GDDR5 MODE SELECTION

MODE	DEF	MODE1	MODE2
0	0	0000	0000
1	1	0000	0000
2	2	0000	0000
3	3	0000	0000

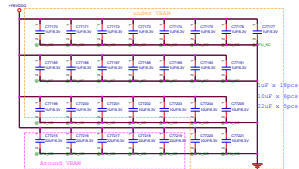
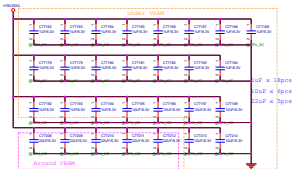
Channel A



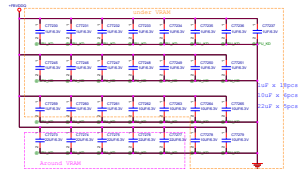
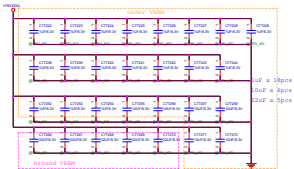
Channel B



Channel C

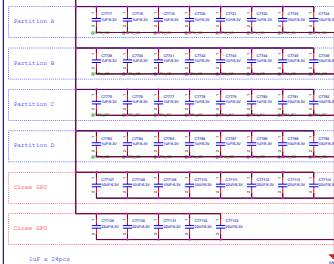


Channel D



VRAM_FWR_FBVDQ

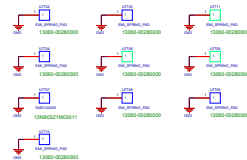
Main Board

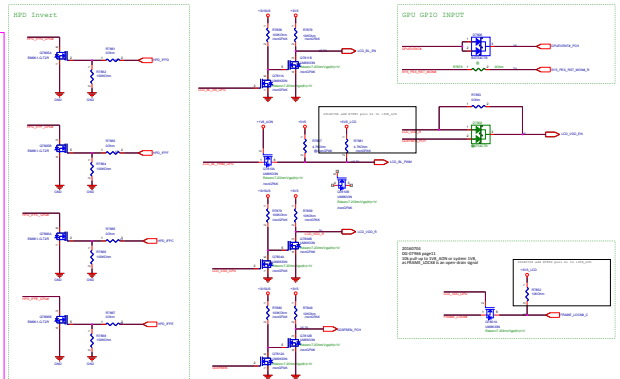
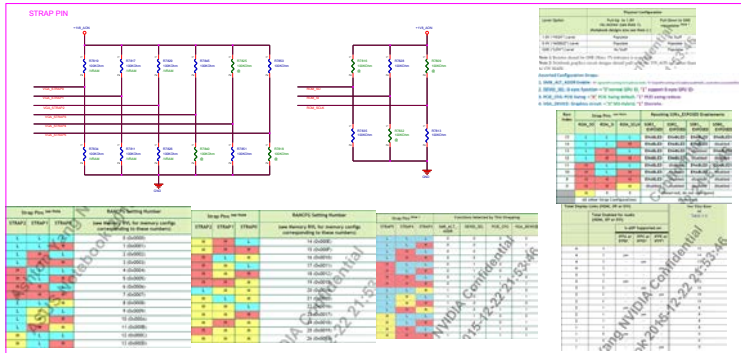
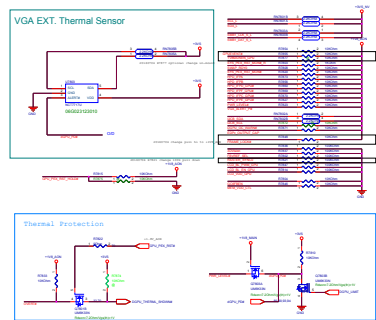
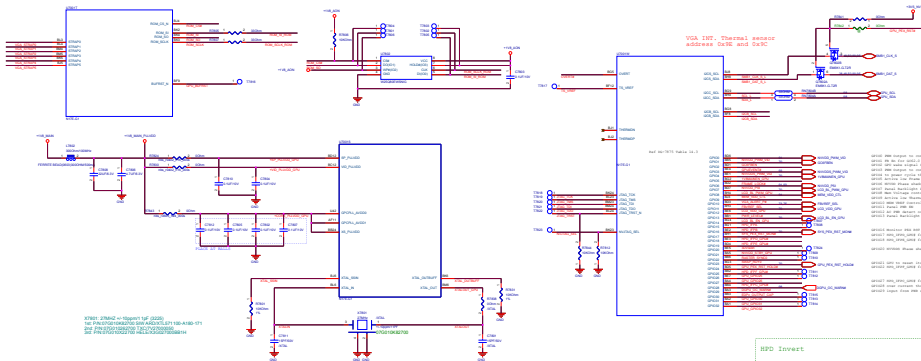


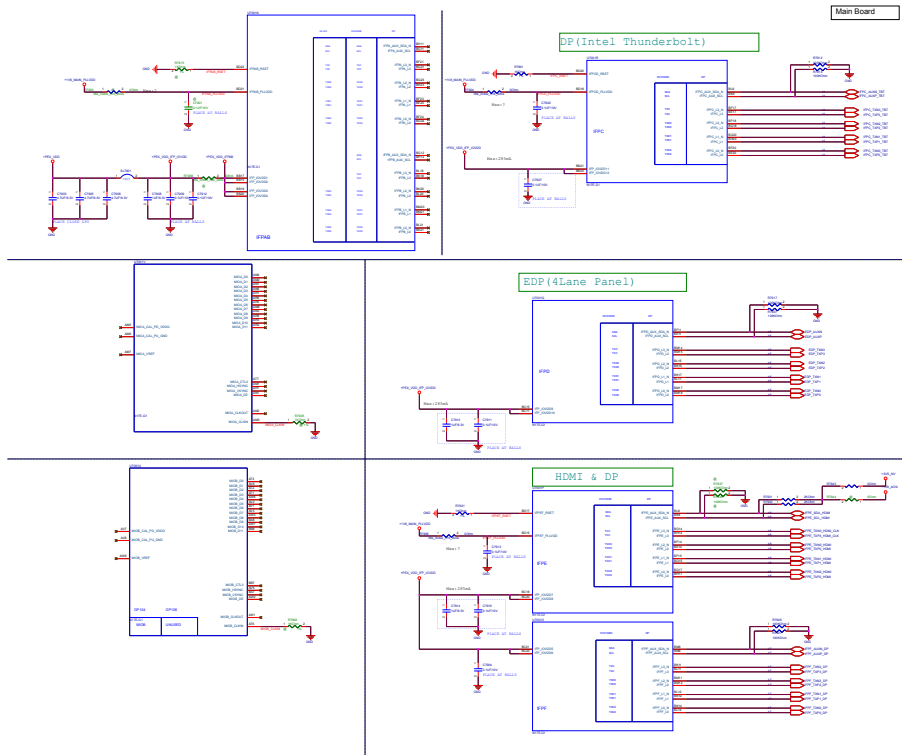
DGPU EMI GND Pad

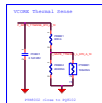
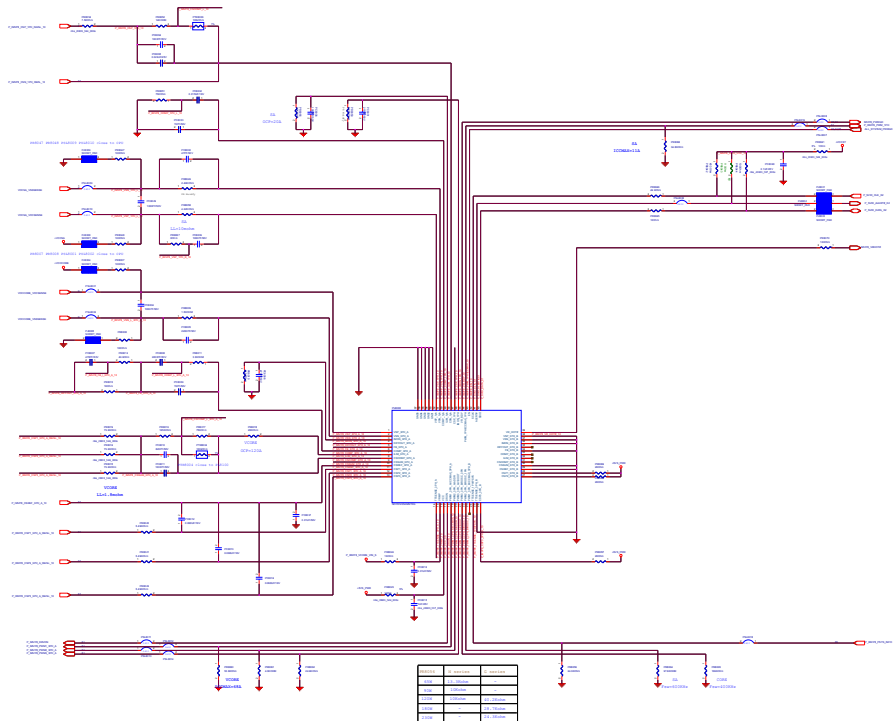
EMI

EMI DGPU Spring

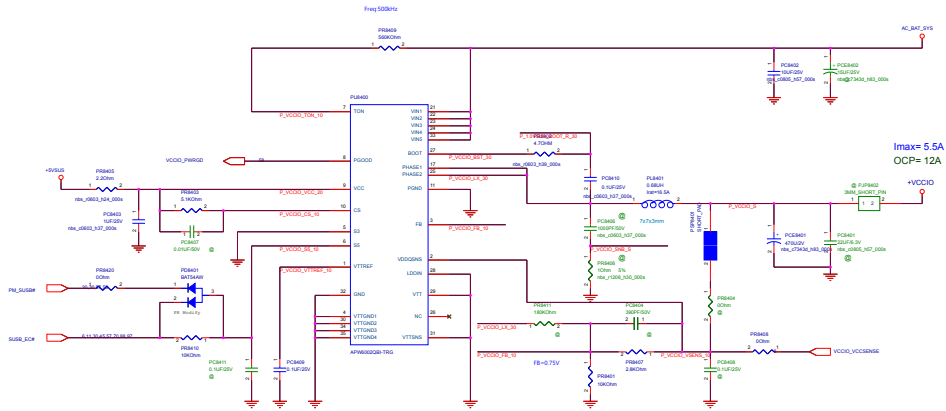


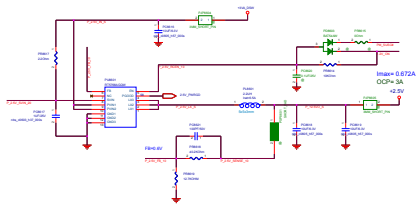
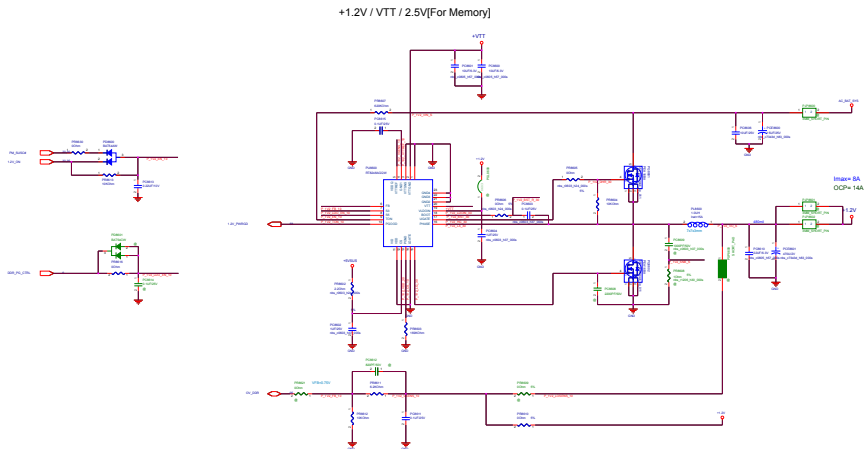


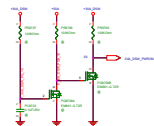
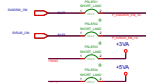
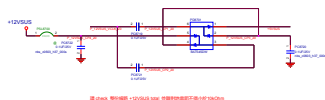






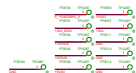




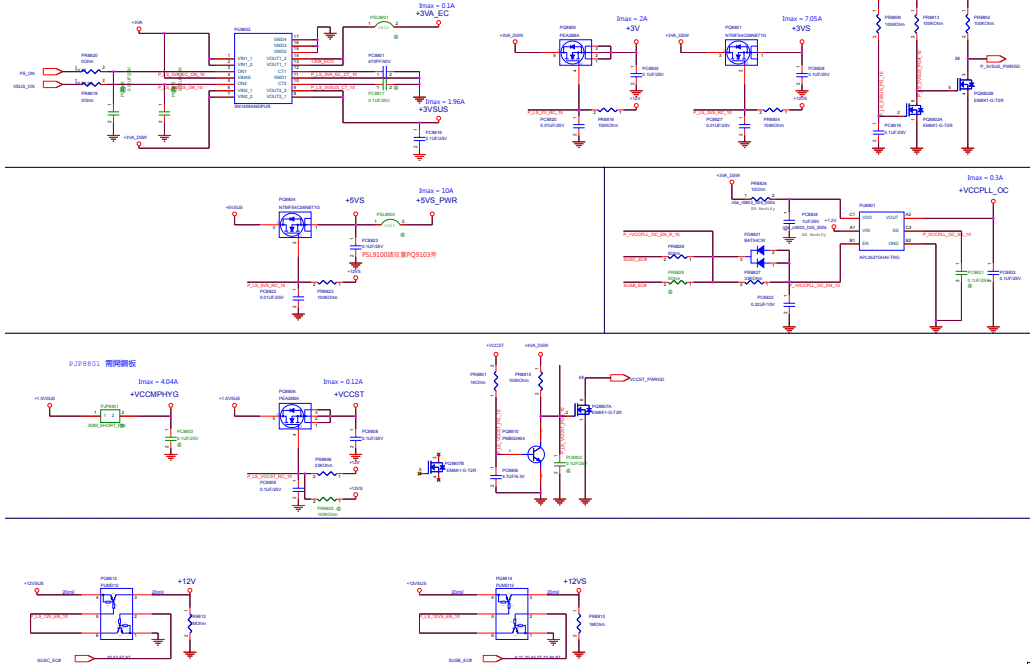


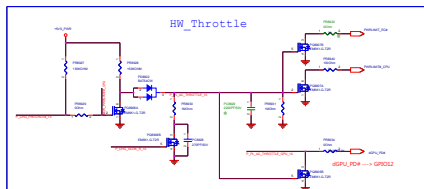
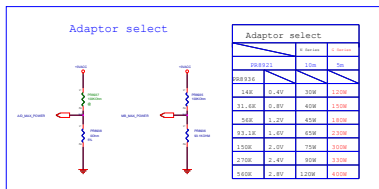
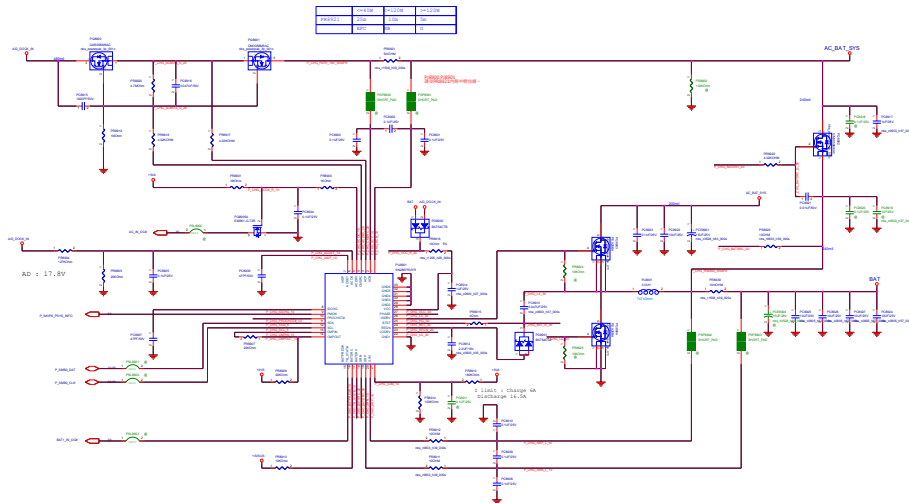
	S0	S18	S3	S60	S6	S6	Bit with USB Charger
PIN_ON	1	-	1	-	1	-	1
Junction_On	1	-	1	-	1	-	1
Output_On	1	-	1	-	0	-	0
Input_On	1	-	1	-	1	-	1
1.8V_On	1	-	1	-	0	-	0
Batt_Rec	1	-	1	-	0	-	0
Batt_ECh	1	-	0	-	0	-	0

	80	05	83	D83	84	85	85 with 0585 Changer
PLD_ON	1	-	-	1	0	0	1
SLAVE_ON	1	-	-	1	0	0	0
OUTL01_ON	1	-	-	0	0	0	0
OUTL02_ON	1	-	-	1	0	0	1
1.20V_ON	1	-	-	1	0	0	0
SLAVE_ROM	1	-	-	0	0	0	0
SLAVE_CMA	1	-	-	0	0	0	0



Load Switch





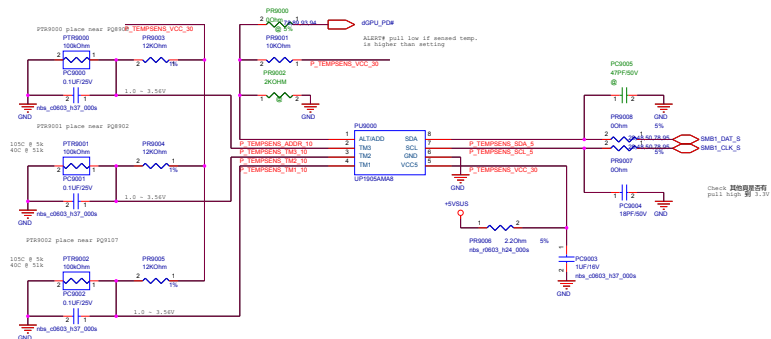
Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x72	0x70
999001	10%	1.5%	2%	3.6%	1.9%	4.3%	5.1%
999002	Open	8.2%	6.2%	6.8%	4.7%	3.6%	2.7%

Register Address

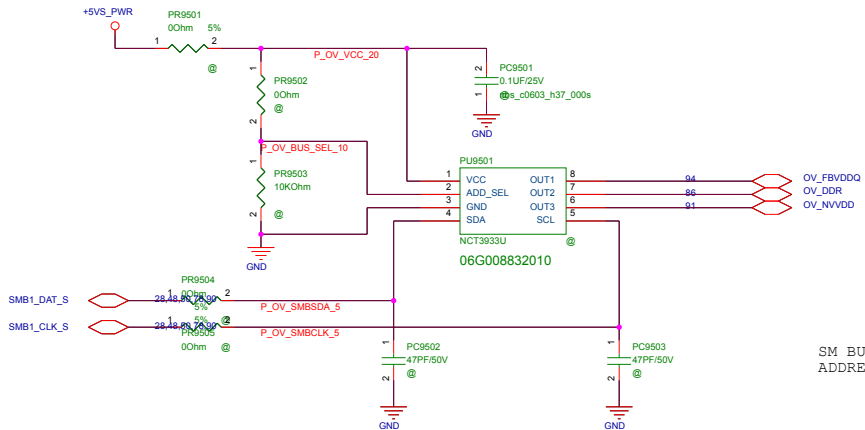
Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

Main Board






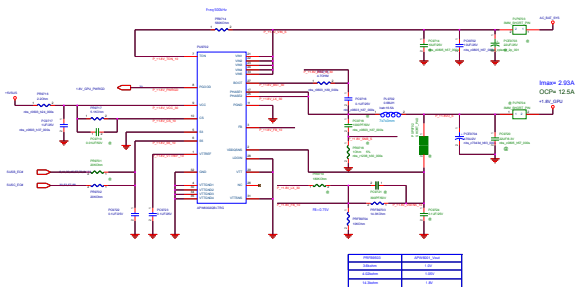
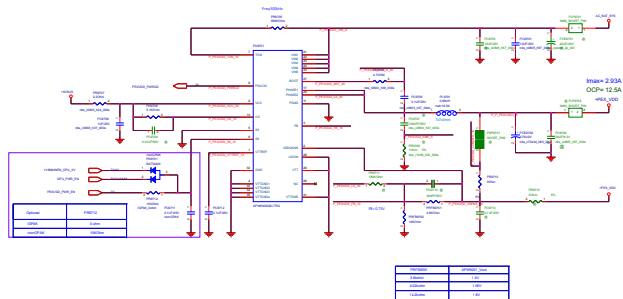


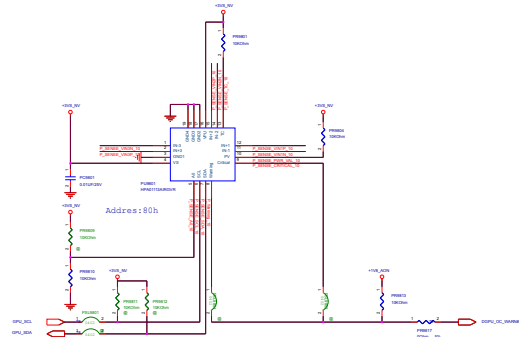
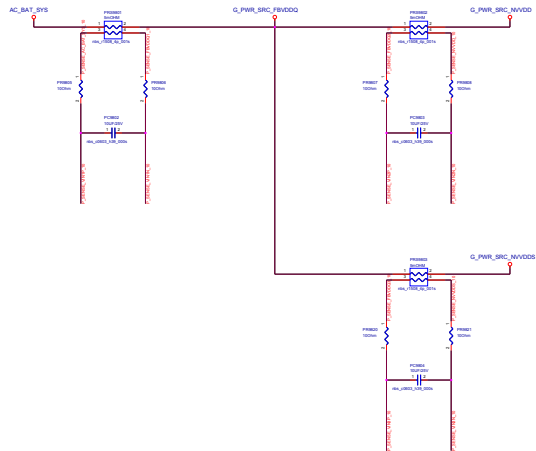


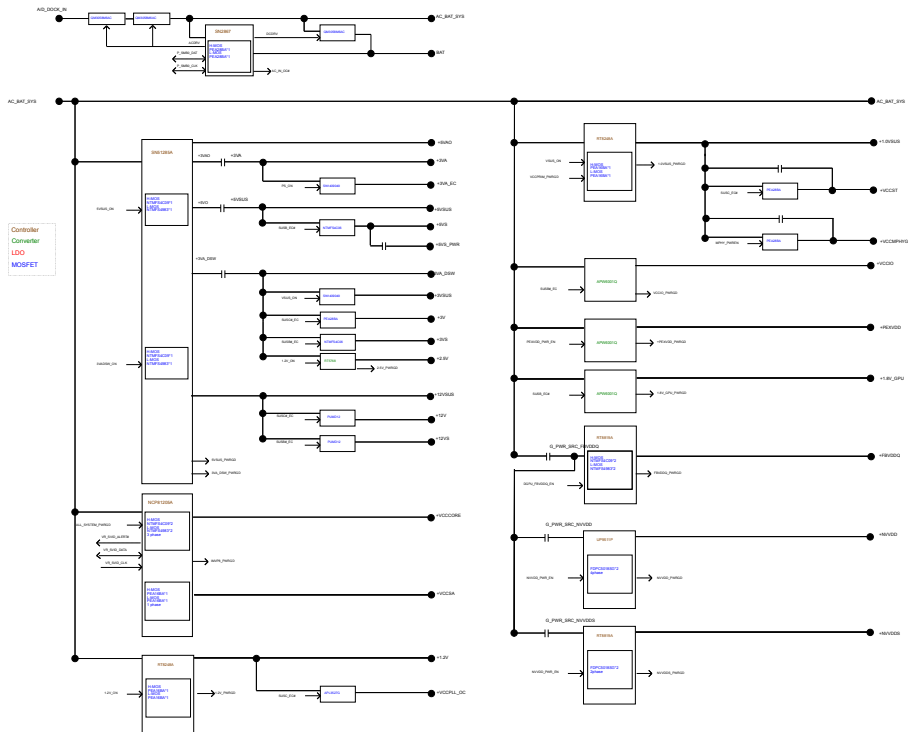
SM BUS SLAVE
ADDRESS:0X2A

<Core Design>

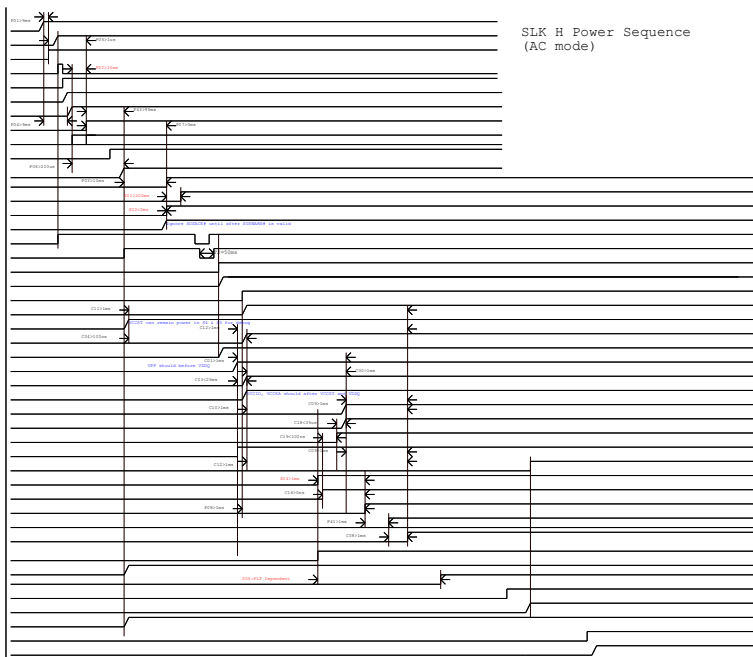
		Project Name	Rev
		G752VSK	R2.0
Title : PW_OV			
Size A	Dept.: NB Power team	Engineer: Benson	
Date: Wednesday, October 12, 2016	Sheet	95	of 102



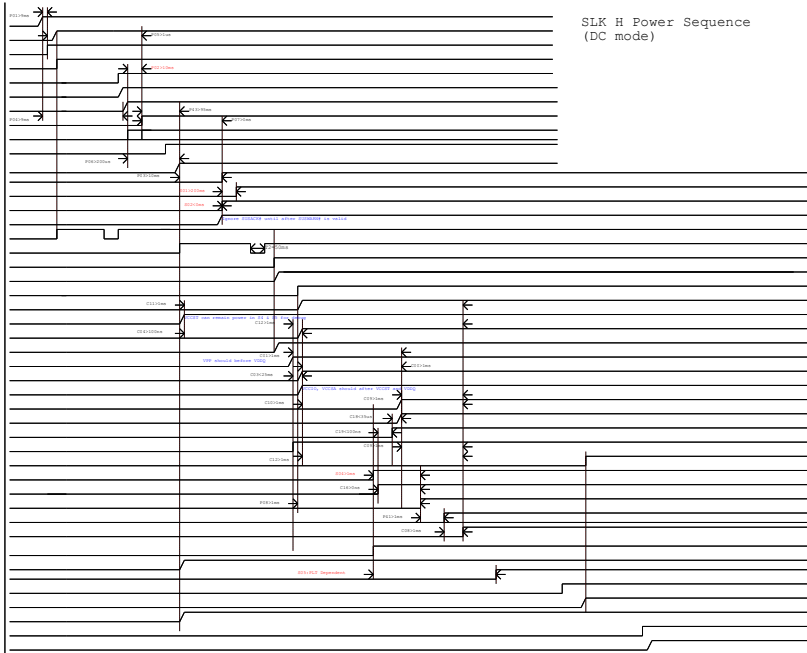




AC-IN Mode

SLK H Power Sequence
(AC mode)

DC-IN Mode

[illegible]SLK H Power Sequence
(DC mode)